Subj: [P1394.1]: Link compatibility with proposed cycle clock adjustment
Date: 98-07-13 10:41:34 EDT
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Background:

The p1394.1 working group has determined that a fast-response feedback mechanism is needed for a non-root node to provide cycle time correction information to the current root. This is based on the following assumptions based on extensive discussions within the group:

1) Different busses connected together with bridges must have cycle times that have a constant long term phase difference, and limited short term phase difference. This is needed to make bridging of isoch data relatively simple and reliable.

2) The desirable clock architecture is hierarchical, with a clock tree constructed out of the interconnected busses, with each two port bridge having a clock slave portal and a clock master portal (there is still discussion of multiple bridges between busses ... in that case, only one bridge would have this kind of slave/master pairing).

3) It is not possible, nor even desirable, to force a bridge node to be the root. Therefore, it is not possible to build a bridge where the "clock master" function could be as simple as directly varying the cycle clock. Instead, we need a communication path to the root of the bus that has the clock master portal.

4) Using a standard aysnch write transaction is not desirable because the latency of the correction could be so long that the correction "amplitude" (the number of 24.576 MHz cycle clock "tics" required to be added or subtracted from the root's cycle clock) would be too high.

5) Using a standard isochronous channel to carry the correction on each isoch interval is undesireable because it uses up a precious resource (an isoch channel).

6) Using a standard asynch write request, but using isoch arbitration is not desireable since a standard 1394-1995 root may try to send an ack ... and using a broadcast address can cause nodes to be flooded with packets that have to be filtered in software.

Problem:

All the proposed solutions to this require violating the letter of the 1394-1995 stndard. They may, however, be fully compatible with existing and planned implementations. The working group would like to find out which of the following proposals may cause problems and which seem easier to implementors for the future:

1) The bridge can send an "ack" packet to the cycle master as a response to a cycle start. The bridge would arbitrate using isochronous mode, just as it

would for an isoch packet. There would be two different acks: "speed up" and "slow down" (codes TBD), which would cause the cycle master to take one fewer or one greater 24.576 MHz clock tic in the current cycle.

2) The bridge will send an "illegal" packet as a response to a cycle start, once again using priority mode. The illegal packet could have a non-standard length (like two bytes), or some other encoding that would be rejected by a standard link (such as an inverted CRC or an illegal tcode).

Please direct all discussion of this to the p1394.1 reflector <stds-1394-1@ieee.org>, or, if you are not a member, back to me and I will forward it for you.

Thank you.

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