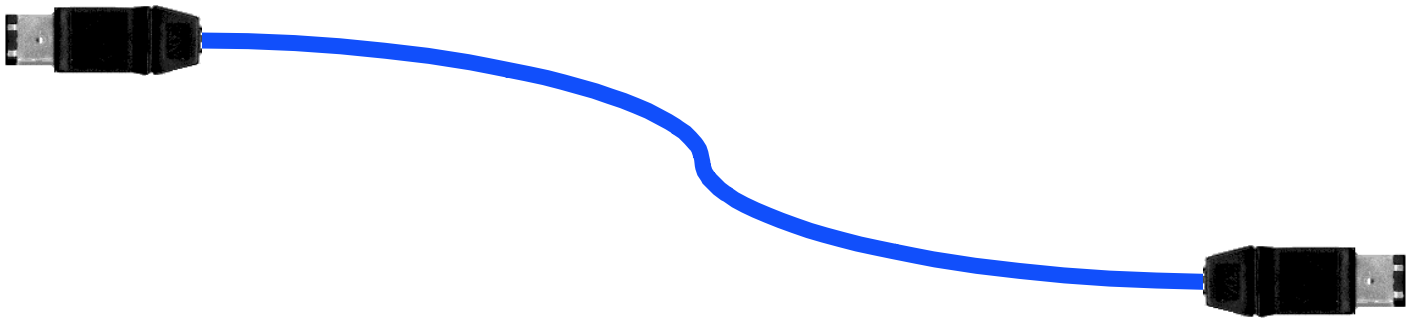
Synchronizing Cycle Master to External Timing Information via Cycle Slave



Solution to Cycle Master Location Limitation

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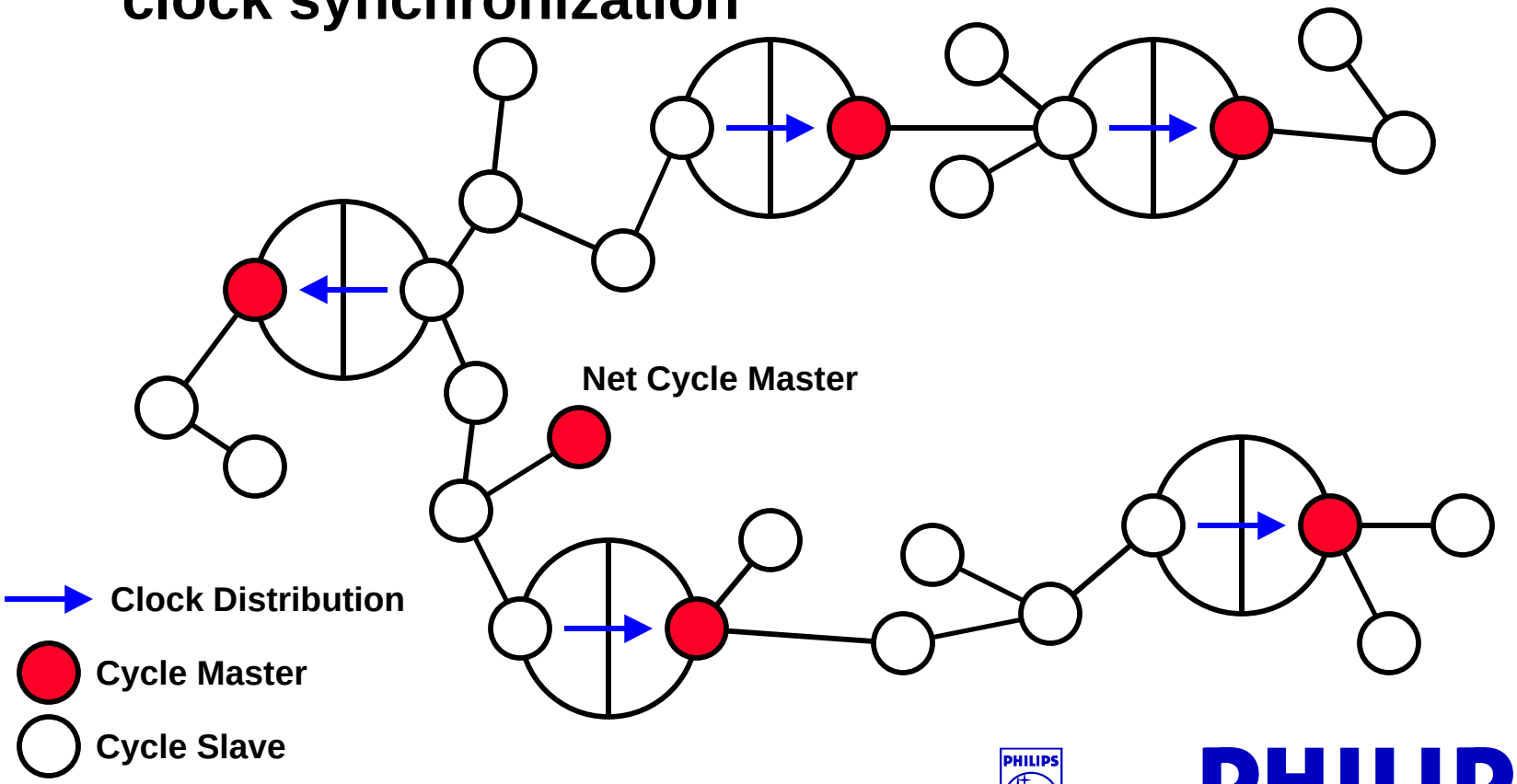
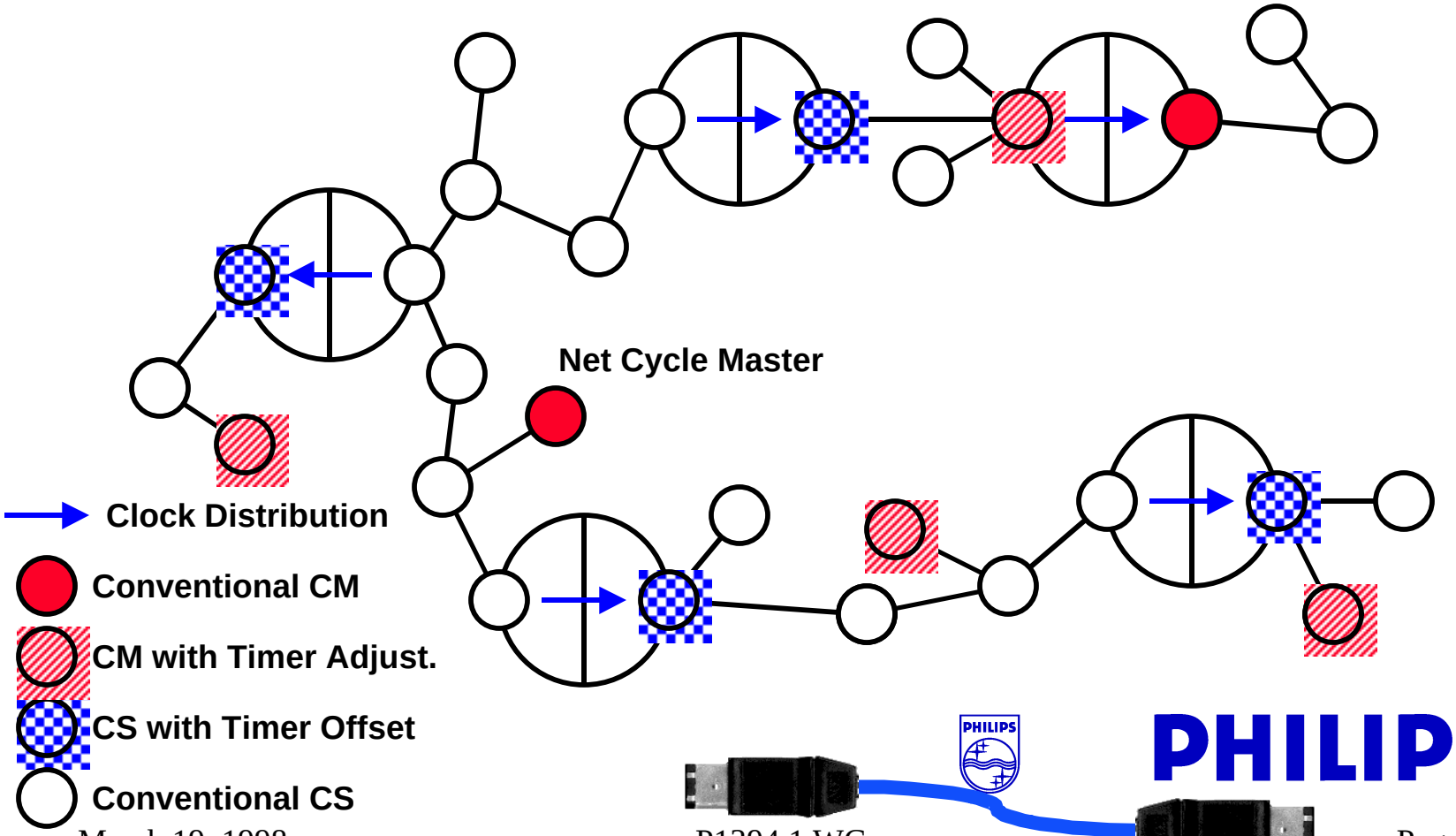
Review - Current Limitation

- **At least one of the portals of each Bridge has to be Cycle Master (root) to ensure network wide clock synchronization**



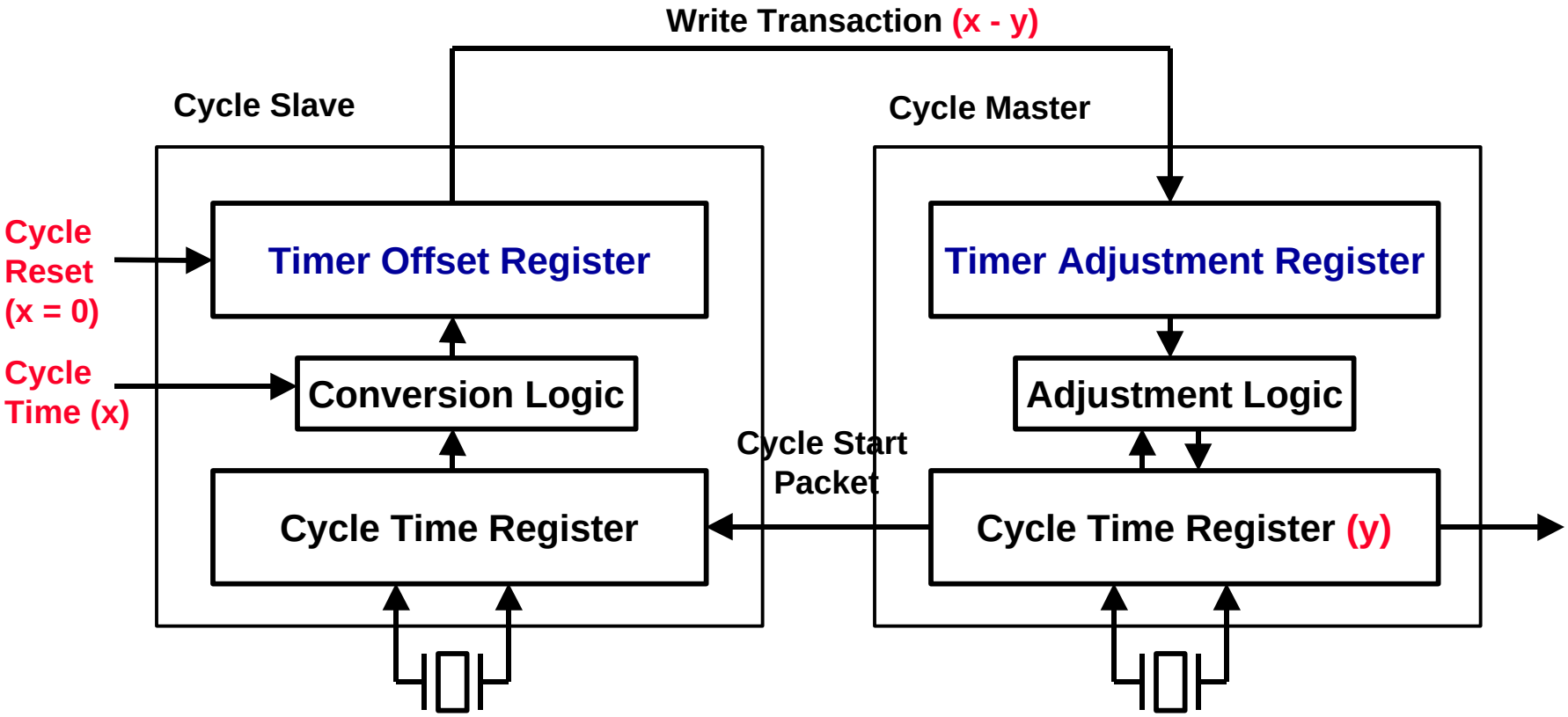
Review - Solution

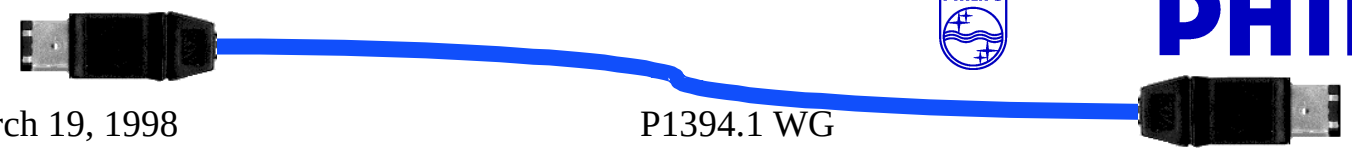
- **Timer Offset/Adjustment Registers provide Full Flexibility of Cycle Master Location on each bus**



Timer Offset Register & Timer Adjustment Register

Feedback Loop!





What Needs to be Standardized?

- **Timer Adjustment Register needs to be standardized**
  - **Location**
  - **Definition**
- **Timer Adjustment Capability Entry in Configuration ROM needs to be standardized**
- **Timer Offset (delta value) can be calculated in various ways**
  - **Definition of delta value can be derived from the definition of Timer Adjustment Register**
  - **No need to standardize Timer Offset Register**
  - **But, it is still a good idea to implement Timer Offset Register in new LINK chips**

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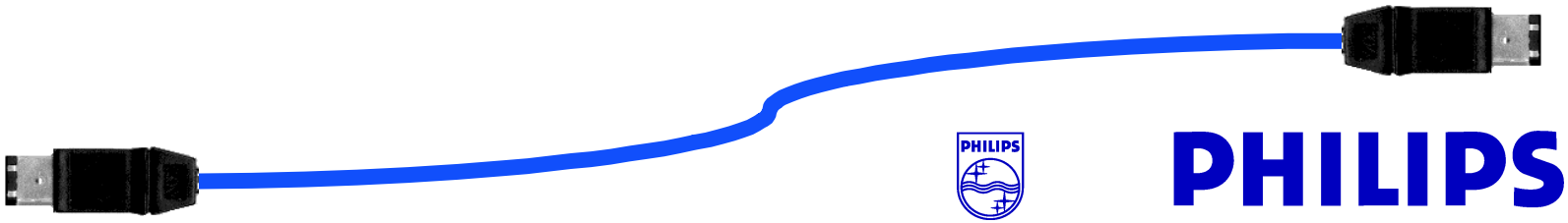
Timer Adjustment Register - Definition (1)

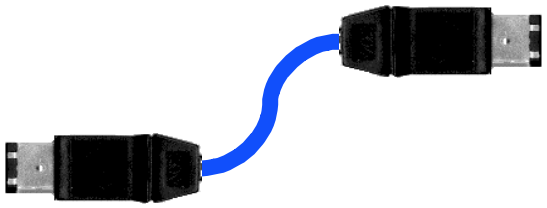
- **delta_cycle_count (Write Only)**
  - 7 bit 2's complement value: range [-64, 63]
  - possible effect on cycle_count and second_count fields of Cycle Time Register
- **delta_cycle_offset (Write Only)**
  - 13 bit 2's complement value: range [-3071, 3071]
  - possible effect on cycle_offset, cycle_count, and second_count fields of Cycle Time Register



Timer Adjustment Register - Definition (2)


```
cycle_offset +=  delta_cycle_offset;
if (cycle_offset >= 3072){          // cycle_offset shall be treated as 14bit integer
    cycle_offset -= 3072;
    cycle_count++;
} else if (cycle_offset < 0){
    cycle_offset += 3072;
    cycle_count--;
}
cycle_count += delta_cycle_count;
if (cycle_count >= 8000){           // [8000, 8095]
    cycle_count -= 8000;
    second_count++;
} else if (cycle_count < 0){        // [8096, 8191] == [-96, -1]
    cycle_count += 8000;
    second_count--;
}
```

NOTE: Delta Values have the opposite polarity from the ones shown in the previous proposal !



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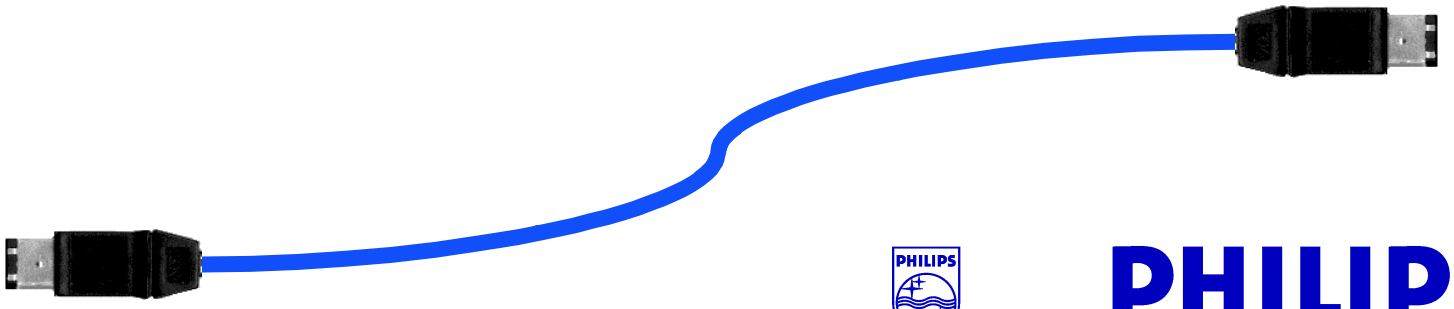
Timer Adjustment Register - Address

- **Proposed Address: 0xFFFF F000 0214**
  - **First reserved address in Serial Bus-Dependent Register Space**
  - **The closest you can get to Cycle Time Register (offset: 0x0200)**
- **Both fields can be written at once, but also each field can be accessed individually**
  - **Other field shall be set to all zeros -> No effect**



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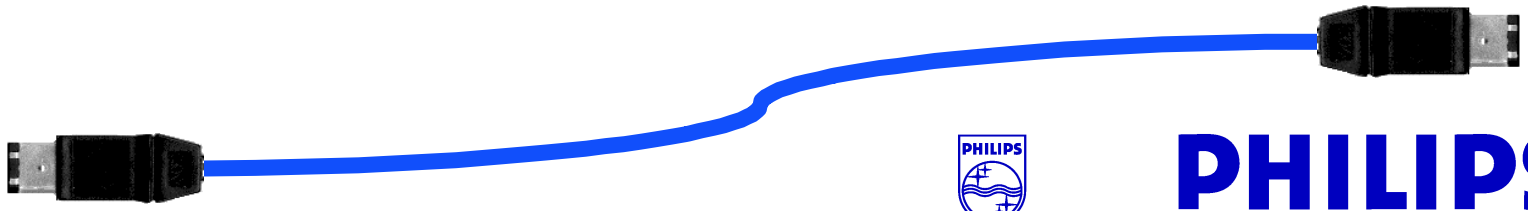
Clock Synchronization Procedure (1)

- During bridge initialization, the whole Cycle Time Register of Cycle Master (CM) is updated by Responsible Bridge Portal (RBP)
- RBP receives Global Time (x) from the other portal and Local Time (y) from Cycle Master (CM)
- delta_cycle_offset can be calculated as

  $(x_{cycle\_offset} - y_{cycle\_offset})$ or

  $(-y_{cycle\_offset})$ when $(x_{cycle\_offset} = 0)$ (use of cycle reset pulse)
- Regular feedback of delta_cycle_offset from RBP to CM is initiated -> cycle_offset locks in



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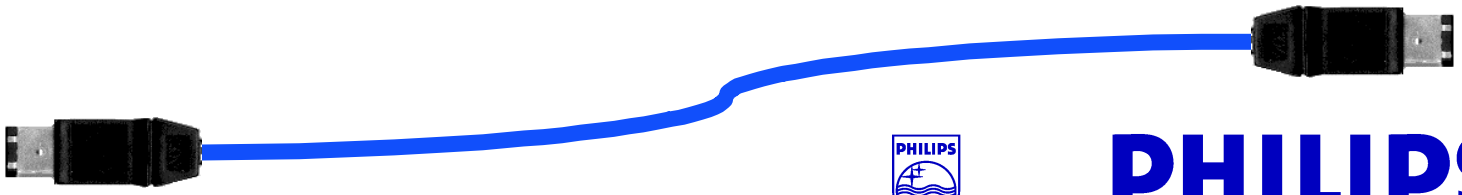
Clock Synchronization Procedure (2)

- **delta_cycle_count can be calculated and fed back to CM at the same time as delta_cycle_offset but the following procedure will be a better choice if cycle reset pulse is used for delta_cycle_offset**
- **delta_cycle_count is calculated by RBP as (x_{cycle_count} - y_{cycle_count}) when cycle_offset is not near the edge (0 or 3071)**
- **delta_cycle_count may be checked every second or occasionally**



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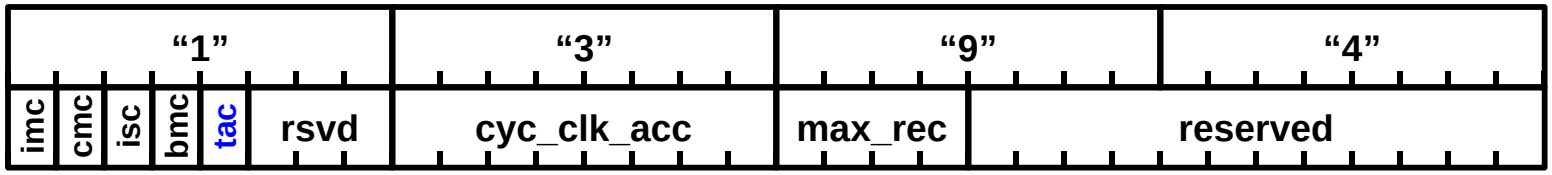
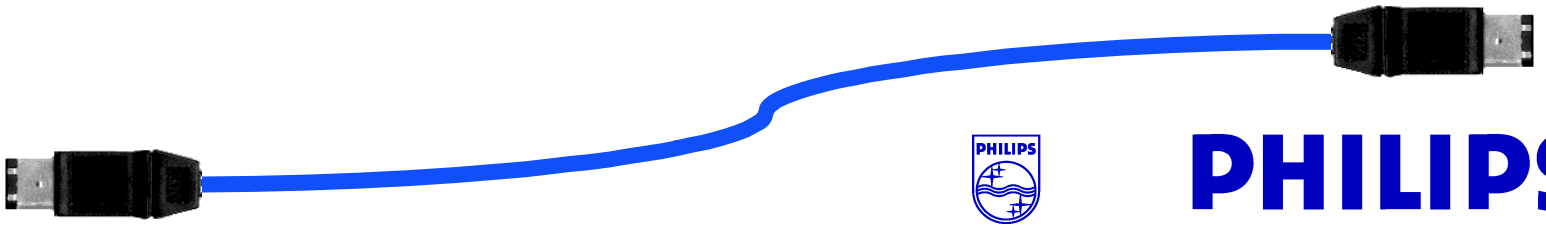
Timer Adjustment Capability Entry



- **In Bus Info Block, 2nd Quadlet (address: 0xFFFF F000 0408)**
- **tac: Timer Adjustment Capable bit**
  - **Implements Timer Adjustment Register as defined in this proposal**



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Conclusion

- **You can start implementing Timer Adjustment Register in your silicon if everybody is happy with this proposal**
- **This proposal needs to be accepted by 1394a Group**
- **Higher-layer protocol shall be defined**
- **More complete proposal (incl. Higher-layer protocol) will be presented at next P1394.1 meeting**