Capabilities Changes to 1394 Specification

Simple 1394 devices may not need to implement all the registers currently required by the 1394 specification. A simple device that is only a slave (i.e., never initiates a transaction) may be quick enough to satisfy all read and write requests without having to split the transaction and, therefor, should not need a SPLIT_TIMEOUT register. The changes that are required in the spec to allow such a device are given below.

Section 8.3.1.2

Change:

d) implement the STATE_CLEAR, STATE_SET, NODE_IDS, RESET_START, and SPLIT_TIMEOUT registers

to:

d) implement the STATE_CLEAR, STATE_SET, NODE_IDS, and RESET_START registers

8.3.2.5.5.2 Node_Capabilities entry

This section defines the fields that must be implemented in a 1394 node. These capabilities do not apply to a simple device that can not initiate bus transactions. The only fields required by a slave device are *64* and *fix*.

Request replacing portion of this section from fourth paragraph (begins, "The 24-bit ***node_capabilities***…") through end of section. Proposed new wording is:

"The 24-bit node_capabilities field contains subfields defined within clause 8.4.11 of ISO/IEC 13213: 1994. Serial Bus node that fully support split transactions shall implement the *spt, 64, lst and drq* bits.

"Split transaction-capable nodes shall set the *spt* bit to one to indicate that the SPLIT_TIMEOUT register is implemeted. Nodes that are not split transaction capable do not need to implement the SPLIT_TIMEOUT register and will set *spt* to 0. If a transaction capable node meets all of the the following criteria, it is not required to implement the SPLIT_TIMEOUT register

a) Shall not initiate a Serial Bus transaction
b) Shall not return ack_pending to any write request
c) Shall complete all read or lock requests with a concatenated response
d) Shall not retry responses under any circumstances

"Transaction-capable node that initiate Serial Bus transactions shall set the *lst* and *drq* bits to one. The lst bit indicates that the STATE_CLEAR.lost bit is implemented. The drq bit indicates that the STATE_CLEAR.dreq but is implemented. The STATE_CLEAR.dreq bit, if cleared by another node, inhibits the initiation of Serial Bus transactions, either asynchronous or isochronous.

"All Serial Bus nodes shall set the *64* and *fix* bits to one."