MACRO Designs

PHY-Link Questionnaire

	PHY	Link
Is status interrupted before all 4 bits are sent	Yes: Fuji, SGST, IBM200, TI No: IBM400	Yes: Fuji, TI, IBM(?) No:
Are transmitted bits cleared as soon as they are sent?	Yes: Fuji, IBM, TI No: SGST	Yes: Fuji, TI, IBM(?) No:
Are all the status bits re-sent or just the bits that could not be sent in the first attempt?	All four: Fuji, SGST, TI Partial: IBM200	All four: IBM Japan Partial:
If a register read is interrupted, are all 16 bits re-sent or just the 12 register bits?	12: IBM200 (partial) 16: Fuji, SGST, IBM400, TI	12: 16: Fuji, TI, IBM(?)

MACRO Designs

PHY-Link Status Abort Recommendations for 1394A

- PHY
  - » Status transfer
    - – always send all four status bits together. (First four bits should not be interrupted)
  - » Register Read
    - – can be terminated anytime after sending the first four status bits
    - – always re-send all 16 bits (4 status and 12 register read)
  - » Status Clearing
    - – clear the status bits after they are sent to the link (This would prevent sending the same status twice)

MACRO Designs

PHY-Link Status Abort Recommendations for 1394A

- Link
  - » Status transfer
    - – Should latch any status bits sent whether the status transfer is terminated or not
    - – Should not expect a re-transfer of interrupted status
  - » Register read
    - – Should latch any status bits sent
    - – Expect a re-transfer of all 16 bits in case of an interruption