MACRO

Designs

PHY - Link Interface Inter-operability Issues and Proposal for P1394A

PHY-Link Questionnaire

	PHY	Link
Is status interrupted before all 4 bits are sent	Yes: Fuji, SGST, IBM200, TI No: IBM400	Yes: Fuji, TI, IBM(?) No:
Are transmitted bits cleared as soon as they are sent?	Yes: Fuji, IBM, TI No: SGST	Yes: Fuji, TI, IBM(?) No:
Are all the status bits re-sent or just the bits that could not be sent in the first attempt?	All four: Fuji, SGST, TI Partial: IBM200	All four: IBM Japan Partial:
If a register read is interrupted, are all 16 bits re-sent or just the 12 register bits?	12: IBM200 (partial) 16: Fuji, SGST, IBM400, TI	12: 16: Fuji, TI, IBM(?)

PHY-Link Status Abort Recommendations for 1394A

MACRO Designs

- ● PHY
  - » Status transfer
    - – The PHY initiates a status transfer if any one of the four status bits is set
    - – When a status transfer is necessary, the PHY always attempts to send all four status bits to the link
    - – Transfer of the four status bits may be interrupted by the phy in case of a 'received_data' indication
    - – The PHY shall clear each status bit after it is sent to the link or if the condition that set the status bit no longer exists

PHY-Link Status Abort Recommendations for 1394A

- **PHY**
  - » **Register Read**
    - – A register read may be interrupted by the phy in case of a 'received_data' indication
    - – If a register read is interrupted, the phy shall re-send all sixteen bits to the link

PHY-Link Status Abort Recommendations for 1394A

- ● **Link**
  - » **Status transfer**
    - – The link shall latch any status bits sent whether the status transfer is interrupted or not
    - – A re-transfer of interrupted status will only occur if any of the four status bits in the PHY are still set
  - » **Register read**
    - – The link shall latch any status bits sent
    - – Expect a re-transfer of all 16 bits in case of an interruption
      - ● Note: The status bits may have changed since the last attempted read register transfer