5.3 AC timing

Figure 5-13 illustrates the Link to PHY transfer waveform at the Link. Figure 5-14 ilustrates the Link to PHY transfer waveform at the PHY. Figure 5-15 illustrates the PHY to Link transfer waveform. The values for the corresponding timing parameters is given in Table 5-25. Link devices shall implement values for td1, td2 and td3 at their outputs which do not exceed the limits specified, and shall not depend on values for tplsu and tplh at their inputs which exceed the limits specified. PHY devices shall implement values for tplsu and tplh at their outputs which at at least meet the values specified, and shall not depend on values for tlpsu and tlph at their inputs which exceed the limits specified. If an isolation barrier is implemented then it shall not cause a delay which exceeds the value specified for idel.

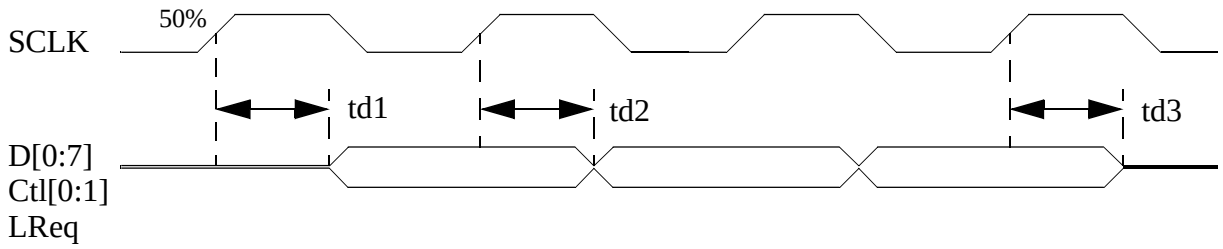

Figure 5-13 Link to PHY transfer waveform at the LINK

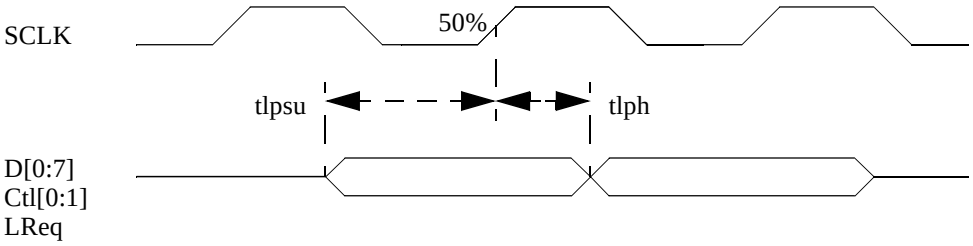

Figure 5-14 Link to PHY transfer waveform at the PHY

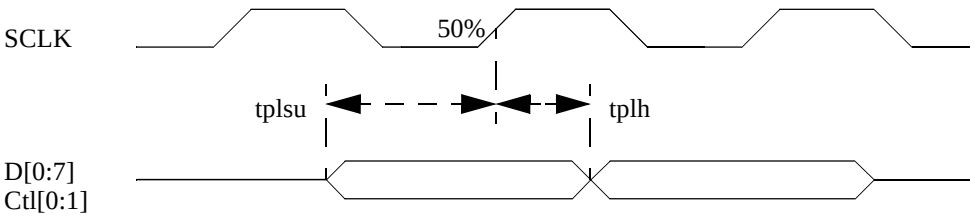

Figure 5-15 PHY to link transfer waveform

Table 1: AC timing parameters

Name	Description	Unit	Min	Nom	Max
tc	SCLK cycle time	ns		20.34	
idel	Delay through isolation barrier (if used)	ns			3
tdl	Delay time, SCLK high to D[0:7], Ctl[0:1] and LReq valid	ns	3		8
td2	Delay time, SCLK high to next value for D[0:7], Ctl[0:1] and LReq	ns	3		8
td3	Delay time, SCLK high to D[0:7], Ctl[0:1] and LReq invalid	ns	3		8
tlpsu	Setup time, D[0:7], Ctl[0:1] and LReq before SCLK	ns	6		
tlph	Hold time, D[0:7], Ctl[0:1] and LReq after SCLK	ns	3		
tplsu	Setup time, D[0:7], Ctl[0:1] before SCLK	ns	6		
tplh	Hold time, D[0:7], Ctl[0:1] after SCLK	ns	0??		
	Hysteresis input rising threshold	V	Vcc/2 +0.2		Vcc/2 +1.3
	Hysteresis input falling threshold	V	Vcc/2 - 1.3		Vcc/2 - 0.2

5.3.1 AC Timing (Informative)

The protocol of this interface is designed such that all inputs and outputs at this interface can be registered immediately before or after the I/O pad and buffer. No state transitions need be made that depend directly on the chip inputs, and chip outputs can come directly from registers without combinational delay or additional loading. This configuration provides generous margins on setup and hold time.

In the direction from the PHY to the Link, the timing follows the normal source clocked signal conventions.

In the direction from the Link to the PHY, the data is timed at the PHY with respect to the SCLK cycle which follows the cycle used to clock the data out of the Link. This allows a nominal budget of 20 ns for various delays, plus the PHY input setup time. The delays allowed for include two delays through a possible isolation barrier (one for SCLK from PHY to Link, one for D[0:7], Ctl[0:7]

and LReq from Link to PHY), and for some delay from the SCLK input at the Link to the Link's registers due to a clock tree. Figure 5-16 illustrates the various delays allowed for. Note that the maximum possible round-trip delay ($tdrt1_{max} = idel_{max} + td1_{max} + idel_{max} = 3 + 8 + 3 = 14$) is used to provide the generous PHY minimum input setup on the next SCLK cycle ($tlpsu_{min} = tc - tdrt1_{max} = 20 - 14 = 6$). Note also that the minimum round-trip delay until the change to the next data ($tdrt2_{min} = tc + idel_{min} + tdl_{min} + idel_{min} = 20 + 0 + 3 + 0 = 23$) limits the hold time at the PHY ($tlph_{min} = tdrt2_{min} - tc = 23 - 20 = 3$).

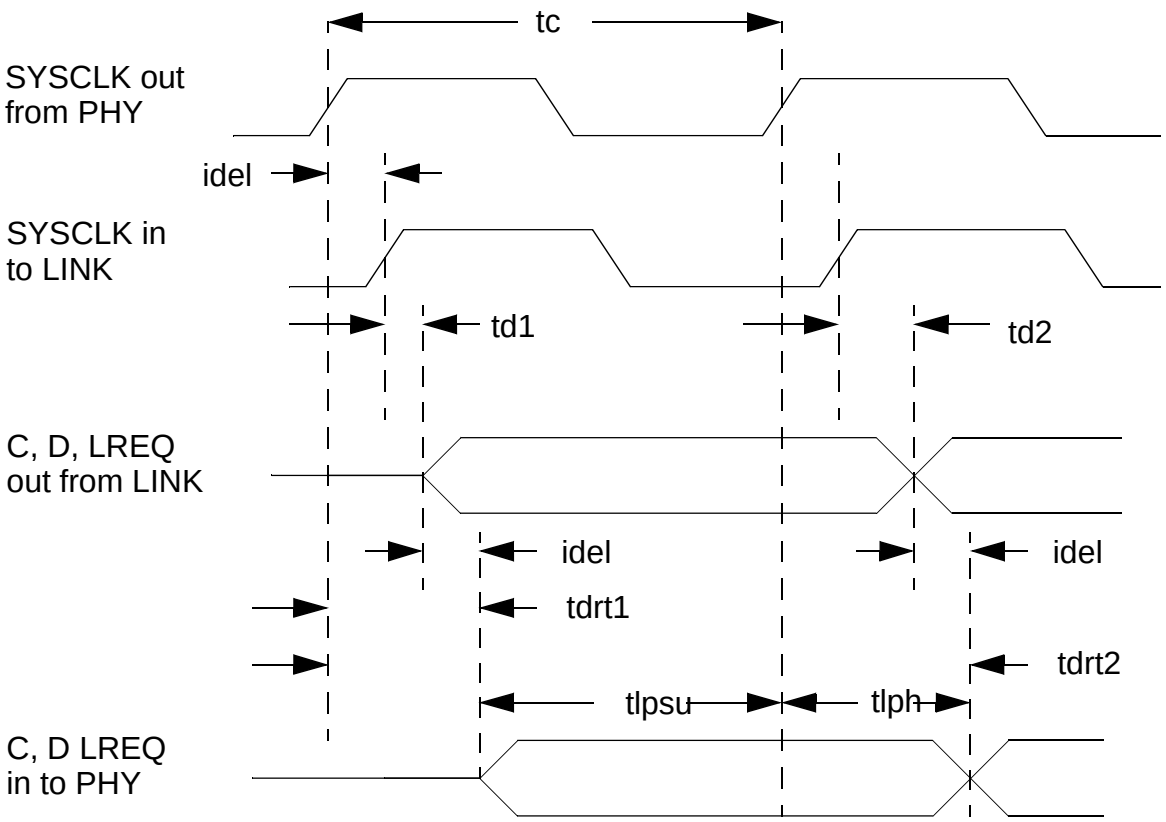

Figure 5-16 Link to PHY delay timings

Table 2: Link to PHY delay timing parameters (informative)

Name	Description	Unit	Min	Nom	Max
tdrt1	Round trip delay from SCLK output at the PHY to valid C[0:1], D[0:7] and LREQ at PHY device	ns	3		14
tdrt2	Round trip delay from SCLK output at the PHY to change or invalid C[0:1], D[0:7] and LReq at the PHY	ns	23		34