5.3 Electrical characteristics of discrete Link/PHY interfaces

This sub-clause applies to the interface provided by discrete PHY or Link devices.

5.3.1 General characteristics

Table 5-9 documents the required DC parametric attributes of all TLL inputs on the PHY-Link interface. The input levels may be greater than the power supply level (i.e., 5V output driving V_{OH} into a 3.3V input), but tolerance to mismatched input levels is optional. Devices not tolerant of mismatched input levels but which otherwise meet the table 5-9 requirements are still regarded as compliant.

5.3.2 Valid signal levels

All AC measurements are made from the 1.4V level of the clock to the valid input or output data levels as shown in figure 5-14.

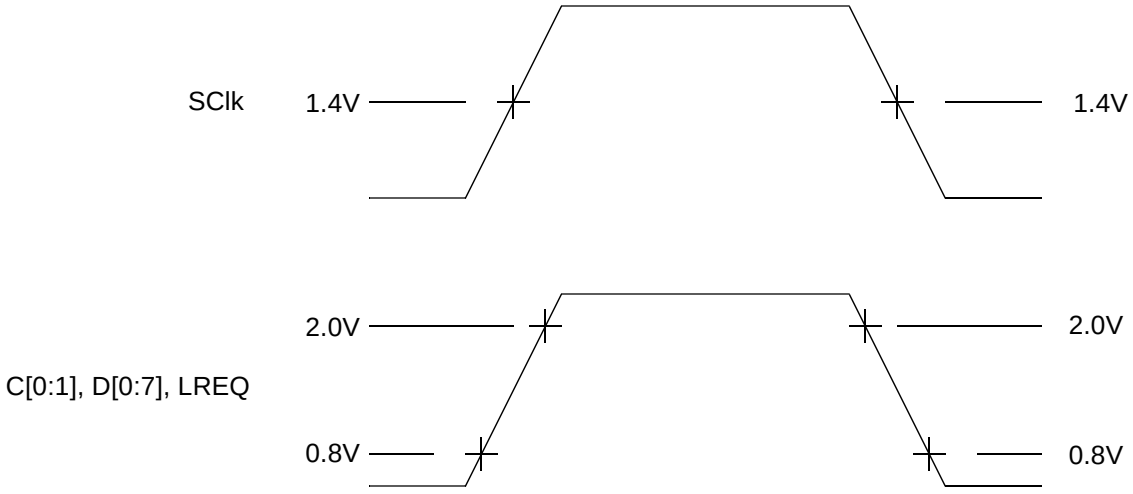

Figure 5-14 — Input output valid levels for AC measurements

Table 5-9 — TTL DC specifications

Name	Description	Conditions		Unit	Minimum	Nominal	Maximum
V_{OH}	Output High Voltage	I_{OH}=-400uA	V_{CC}=Min	V	2.2	3.0	V_{CC}
V_{OL}	Output Low Voltage	I_{OL}=1mA	V_{CC}=Min	V	GND	0.25	0.6
V_{IH}	Input High Voltage			V	2.0		V_{CC}[a]+10%
V_{IL}	Input Low Voltage			V	GND		0.8
I_{IH}	Input High Current	V_{CC}=Max	V_{IN}=2.4V	uA			40
I_{IL}	Input Low Current	V_{CC}=Max	V_{IN}=0.4V	uA			600

Table 5-9 — TTL DC specifications (Continued)

Name	Description	Conditions		Unit	Minimum	Nominal	Maximum
C_{IN}	Input Capacitance			pf			4.0
t_R	Clock Rise Time	0.8V to 2.0V		ns	0.7		2.4
t_F	Clock Fall Time	2.0V to 0.8V		ns	0.7		2.4
t_R	Data Rise Time	0.8V to 2.0V		ns	0.7		
t_F	Data Fall Time	2.0V to 0.8V		ns	0.7		

[a.] Refers to driving device power supply

5.3.3 Rise and fall time definition

The rise and fall time definition for SClk, C[0:1], D[0:7] and LReq is shown in figure 5-15.

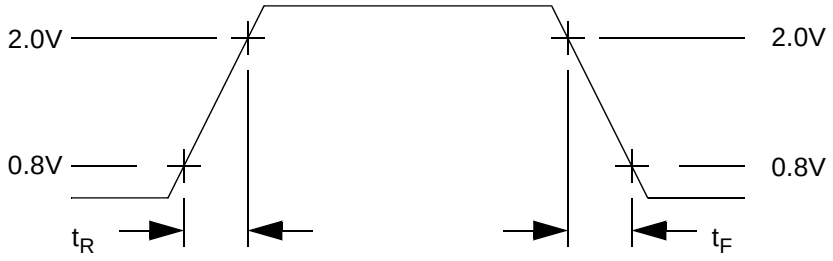

Figure 5-15 — Rise and fall time definition

5.3.4 TTL Load

All AC measurements are assumed to have the output load of 10 pF.

5.3.5 AC timing

Figures 5-16 through 5-18 below illustrate the transfer waveforms as observed at the link and the PHY. A PHY shall implement values for tlsu and tlh (measured at their outputs) of at least the minimum values specified by table 5-11 and shall not depend upon values for tpsu and tph (measured at their inputs) less than the minimum values specified. A link shall implement values for td1, td2 and td3 (measured at their outputs) within the limits specified by table 5-12 and shall not depend upon values for tlsu and tlh (measured at their inputs) less than the minimum values specified. If an isolation barrier is implemented it shall not cause a delay in excess of the value specified for idel, or cause a skew greater than the value specified in table 5-10.

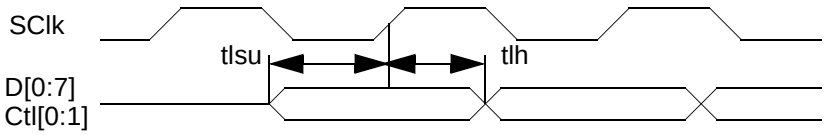

Figure 5-16 — PHY to link transfer waveform

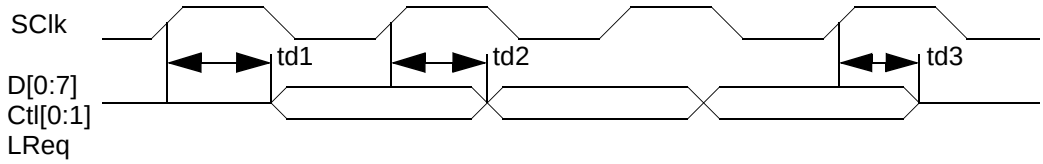

Figure 5-17 — Link to PHY transfer waveform at the link

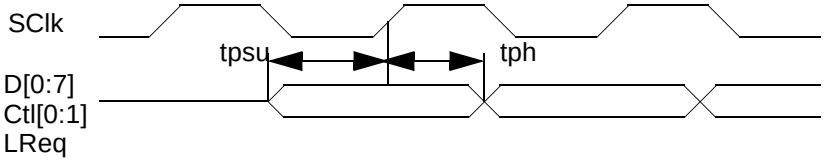

Figure 5-18 — Link to PHY transfer waveform at the PHY

The values for the timing parameters illustrated above are specified in the following table.

Table 5-10 — General AC timing parameters

Name	Description	Unit	Minimum	Nominal	Maximum
tc	SClk cycle time	ns	20.24	20.34	20.45
idel	Delay through isolation barrier	ns			2
	Skew through isolation barrier	ns			0.5
	Hysteresis input rising threshold	V	Vcc/2 + 0.2		Vcc/2 + 1.3
	Hysteresis input falling threshold	V	Vcc/2 - 1.3		Vcc/2 - 0.2

Table 5-11 — AC timing parameters at the PHY

Name	Description	Unit	Minimum	Nominal	Maximum
tpsu	Setup time for D[0:7], Ctl[0:1] and LReq inputs before SClk output	ns	6		
tph	Hold time for D[0:7], Ctl[0:1] and LReq inputs after SClk output	ns	0		
tlsu	Setup time for D[0:7] and Ctl[0:1] outputs before SClk	ns	6.5		
tlh	Hold time for D[0:7] and Ctl[0:1] outputs after SClk	ns	0.5		

Table 5-12 — AC timing parameters at the Link

Name	Description	Unit	Minimum	Nominal	Maximum
td1	Delay time from SClk input high to initial instance of D[0:7}, Ctl[0:1] and LReq outputs from tri-state to active and valid	ns	1		10
td2	Delay time from SClk input high to subsequent instance(s) of D[0:7], Ctl[0:1] and LReq outputs valid	ns	1		10

Table 5-12 — AC timing parameters at the Link (Continued)

Name	Description	Unit	Minimum	Nominal	Maximum
td3	Delay time from SClk input high to D[0:7], Ctl[0:1] and LReq outputs tri-state	ns	1		10
tlsu	Setup time for D[0:7] and Ctl[0:1] inputs before SClk	ns	6		
tlh	Hold time for D[0:7] and Ctl[0:1] inputs after SClk	ns	0		

5.4 AC timing (informative)

The protocol of this interface is designed such that all inputs and outputs at this interface can be registered immediately before or after the I/O pad and buffer. No state transitions need be made that depend directly on the chip inputs; chip outputs can come directly from registers without combinational delay or additional loading. This configuration provides generous margins on setup and hold time.

In the direction from the PHY to the link, timing follows normal source-clocked signal conventions. A 0.5 ns allowance is included for skew through an isolation barrier.

In the direction from the link to the PHY, the data is timed at the PHY in reference to SClk. This allows nominal budget of 20 ns for delay, exclusive of the PHY input setup time. Possible sources of delay are an isolation barrier or internal SClk delay at the link caused by a clock tree. Figure 5-19 illustrates the relationship of these delays. Note that the maximum round-trip delay of 14 ns (calculated as $tdrt1_{max}$ = $idel_{max}$ +$td1_{max}$ +$idel_{max}$) provides a generous link delay from the link receiving SClk to the link providing valid data of 10ns, and a generous PHY minimum input setup for the subsequent SClk cycle of 6 ns (calculated as $tpsu_{min}$ = tc - $tdrt1_{max}$). Also note that the minimum round-trip delay until the next change in data of 21 ns (calculated as $tdrt2_{min}$ = tc + $idel_{min}$ + $td1_{min}$ + $idel_{min}$) limits the hold time at the PHY to 1 ns (calculated as tph_{min} = $tdrt2_{min}$ - tc), which is reduced to 0 ns to provide a guardband of 1 ns.

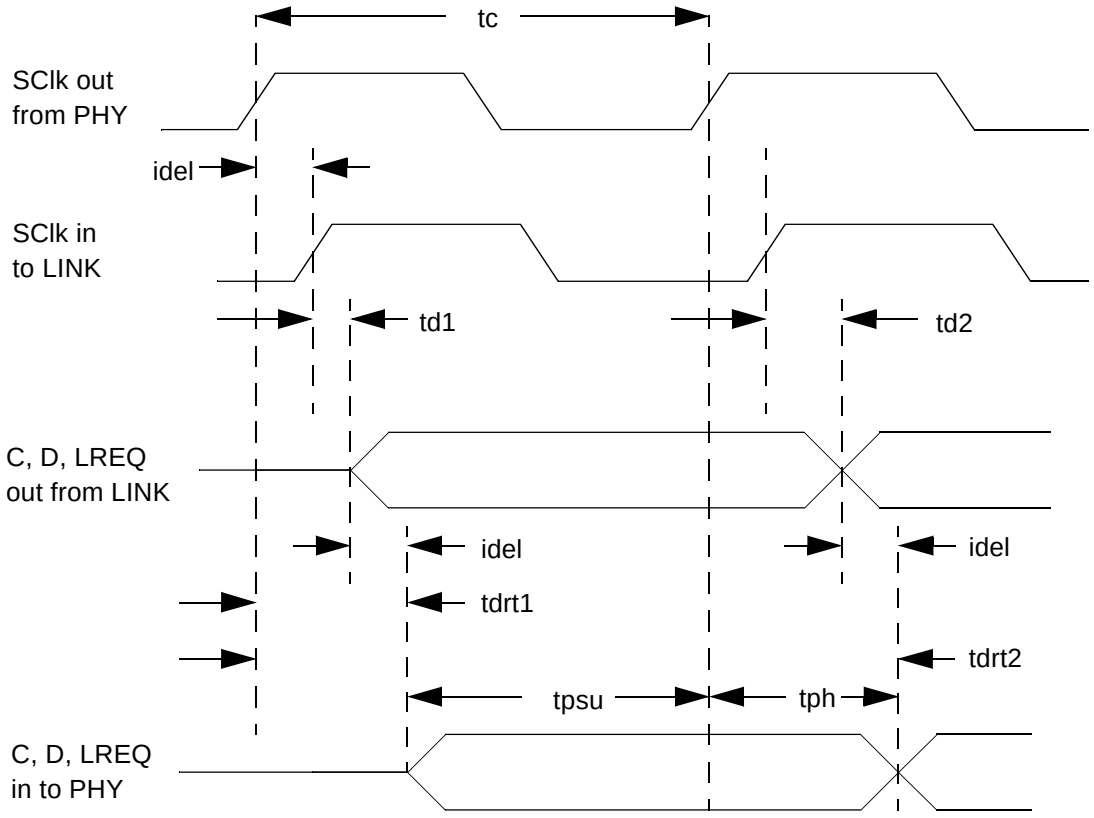

Figure 5-19 — Link to PHY delay timing

The values for the delays illustrated above are given by table 5-13 below.

Table 5-13 — Link to PHY delay timing parameters

Name	Description	Unit	Minimum	Nominal	Maximum
tdrt1	Round-trip delay from SClk output at the PHY to valid Ctl[0:1], D:[0:7] and LREQ at the PHY	ns	1		14
tdrt2	Round-trip delay from SClk output at the PHY to changed or invalid Ctl[0:1], D:[0:7] and LREQ at the PHY	ns	21		34