CONGRUENT SOFTWARE, INC.
3998 Whittle Avenue
Oakland, CA 94602
(510) 531-5472
(510) 531-2942 FAX

FROM: Peter Johansson

TO: IEEE P1394a Working Group

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RE: "Fairness" and Asynchronous Arbitration

This document is a summary of the discussions started by Dave LaFollette at the March 17 - 18 P1394a meeting in San Jose. Subsequent reflector discussions—as well as some calculations by Dave about the maximum useful fairness budget—have refined the proposal.

Because the subject is still being debated I've elected to summarize it rather than immediately place it in the working draft of P1394a. The working group can take a formal decision on this or a modified proposal at the May meeting in Phoenix.

9.x FAIRNESS_BUDGET register

The FAIRNESS_BUDGET register permits the bus manager to configure a node's fair arbitration behavior in order to optimize Serial Bus utilization. The definition is given by figure 9-x below.
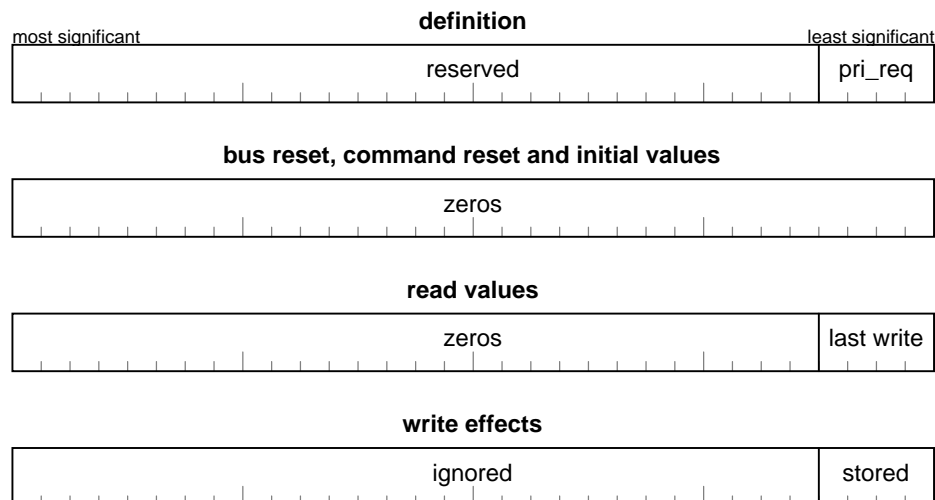

Figure 9-x – FAIRNESS_BUDGET format

The *pri_req* field shall specify the maximum number of priority arbitration requests for an asynchronous request packet that the link is permitted to make of the PHY during a fairness interval. A Serial Bus fairness interval exists between the occurrence of an arbitration reset gap

and the first subsequent arbitration reset gap. The *pri_req* default value of zero is equivalent to the fair arbitration behavior specified by IEEE Std 1394-1995.

Each time a link receives PHY status of ARB_RESET_GAP, it shall reset an internal variable, *priority_request_count*, to the value of *pri_req* from the FAIRNESS_BUDGET register. When the link wishes the PHY to arbitrate for the bus in order to send a packet with one of the transaction codes listed in table 9-x, it may make a priority arbitration request if the value of *priority_request_count* is nonzero. Each time the link makes a priority arbitration request for one of these transaction codes it shall decrement *priority_request_count*.

Table 9-x – Transaction codes valid for priority arbitration

Value	Description
0	Quadlet write request
1	Block write request
4	Quadlet read request
5	Block read request
9	Lock request

The bus manager shall ensure that the sum of the values of *pri_req* in the FAIRNESS_BUDGET registers of all nodes is less than or equal to 63 minus the number of nodes.

NOTE— IEEE Std 1394-1995 specifies only one use for the priority arbitration request from the link to the PHY: to arbitrate for the bus in order to transmit a cycle start packet. This supplement does not change that use of priority request and it shall not count against the *priority_request_count* maintained by the link.