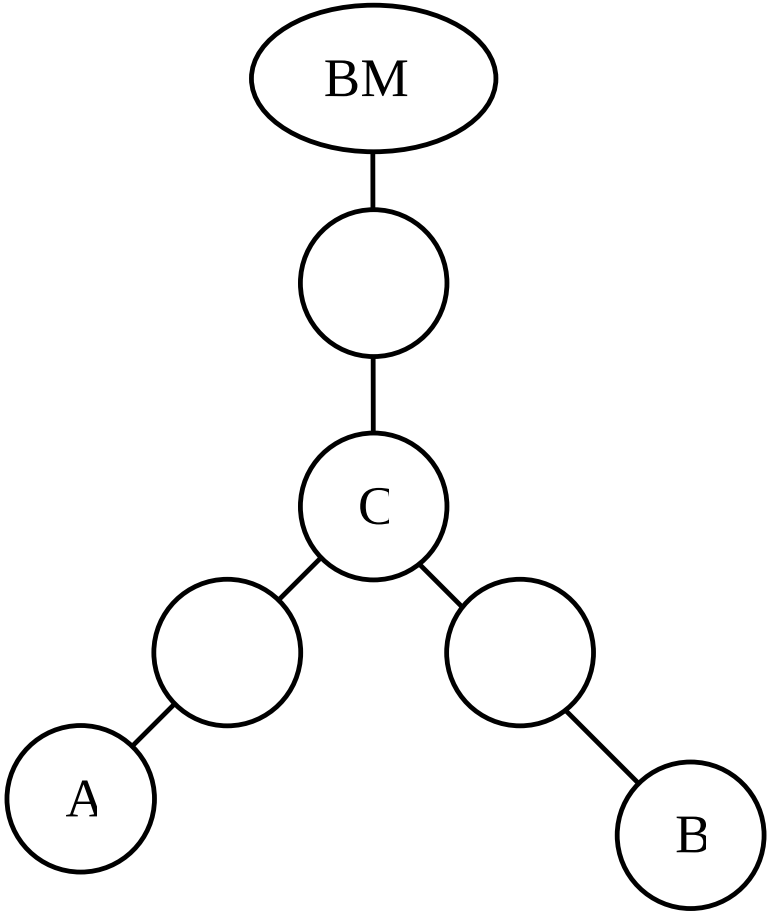
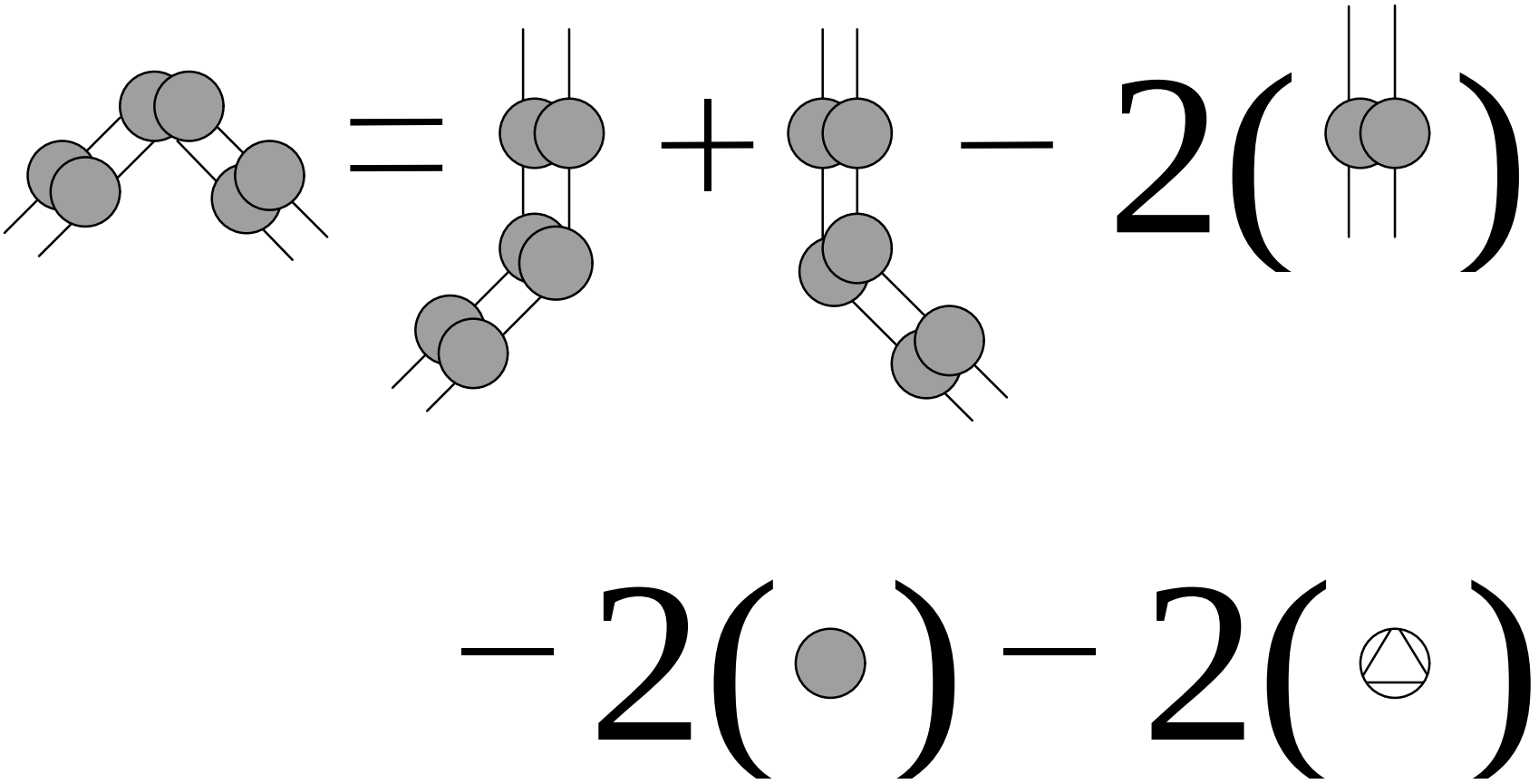
Phy Pinging

Most Complex Topology for Phy Pinging

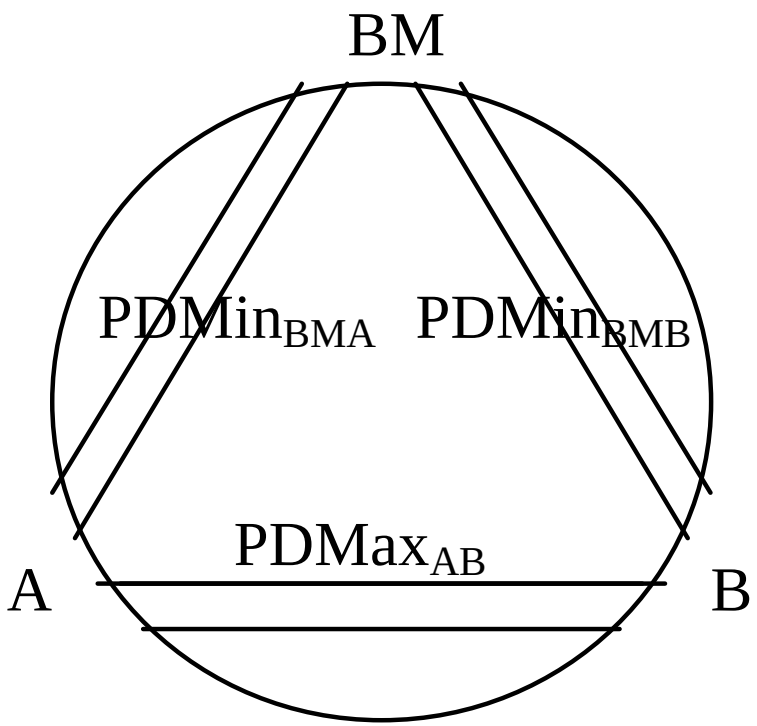


- To determine delays from between A and B the Bus Manager must
  - » Ping node A
  - » Ping node B
  - » Ping node C
  - » Account for jitter and worst case times
  - » Add the delays to A and B
  - » Subtract twice the delays to C
  - » Subtract extra node C Phy Delays
  - » Compensate for differences in port to port Phy delays through node C

Graphical Representation of Round Trip Delay Calculation



Node C Port to Port Phy Delay Compensation



- Measurements include Phy Delays along paths from Bus Manager to nodes A and B
- Phy delay along path from node A to node B is needed
- The difference may be larger in nodes which have 1394B ports.

Proposed New 1394A Constants

Timing constant	Minimum	Maximum
ARB_RESPONSE_DELAY	33.3 ns	PHY_DELAY max
LINK_TO_BUS_DELAY	40 ns	62 ns
PHY_DELAY	100 ns	
PHY_DELAY_JITTER (report?)		20 ns
BUS_TO_LINK_DELAY	81 ns	102 ns
PING_RESPONSE_TIME	122 ns	143 ns

Possible Alternative 1394B Gap Count solution

- Longer cables or Phy delays imply 1394B nodes or subPhys
- 1394B nodes with long cables or Phy delays report them to the Bus manager
  - » Phy or subPhy register read?
  - » Caboose packet?
  - » New Write Request Packets?
- Cable Delay + Phy Delays on both ends are measured during Beta start-up
- Any delay on the parent path above that assumed by the bus manager is reported by the child node
- Phy Pinging exists as back up method