(CWS1) 5.1.1 p38 (T) We should consider requiring backwards compatibility with 1394-1995. It would be a pity if the system designer has to check whether the new PHY can accept his old LINK.

I propose "A PHY shall also accept a 7-bit request as specified in IEEE 1394-1995. (Note, this will be terminated with a 0 stop bit in the same position as LR[6] in the 8-bit request, which is equivalent to LR[6]=0 for S100, S200 and S400 speed requests.)"

(CWS2) 5.1.2 and Table 5-10 p41/42 (E/T) I believe that we agreed in the last meeting on the statements concerning when the various bits are reset.

Add the following (I suggest after Fig 5-3):-

In the event of a packet reception during status transfer, the PHY may prematurely end the transfer by removing the status indication on the CTL[0:1] signals. Any status bits transferred shall be reset, even if the status transfer is prematurely terminated (i.e. if it is terminated after the transfer of S[0:1], then S[0:1] will be reset. If it is terminated after the transfer of S[0:n] where n>=3, then S[0:3] will be reset). The status transfer shall be retried at the next available opportunity if it was a 16 bit status transfer, or if it was a 4 bit status transfer and at least one of the four status bits S[0] to S[3] is (still) 1.

In Table 5-10, for ARB_RESET_GAP and SUBACTION_GAP and subsction gap, the following should be added "This bit shall be reset after the status transfer or when a transfer occurs on the bus." For BUS_RESET_START and PHY_Interrupt the following should be added "This bit shall be reset after the status transfer".

(CWS3) Figure 5-4 p43 (E) The second timing diagram is for "Concatenated Packet", not "Continued Packet"

(CWS4) Table 5-13 p47 (E/T) The relationship between {Pwr_fail, Timeout and Bias_Change} and PHY_Interrupt status bit needs to be made clear. Add to each of the entries "The PHY_interrupt status bit shall be set when this bit transitions from 0 to 1."

(CWS5) Table 5-13 p47 (E) I have had problems with non-native English speakers on the (slightly bizarre) specification for how to reset the Loop, Pwr_fail, Timeout and Bias_Change bits. They interpret a "write of 1 to the bit" as "storing a 1 in the bit". I suggest the slightly more long-winded:-

"A register write with the value 1 in the field corresponding to this bit clears the bit to zero."

(CWS6) Table 5-13 p47 (E/T) Following on from the above, we should clarify in each description for the Loop, Pwr_fail, Timeout and Bias_Change bits:-

"A register write with a value 0 to the field corresponding to this bit has no effect on the bit."

(CWS7) Table 5-13 p47 (T) The new comment at the foot of the table is NOT what we agreed and definitely wrong. If you specify PHY_Interrupt as the logical "OR" of these bits, then it won't be resettable on a Status transfer. The sequence of events is that the transition from 0 to 1 on any of the Loop, Pwr_fail etc bits sets the PHY_Interrupt status, the status transfer to the PHY takes place, the PHY_Interrupt status is reset (if you don't do this, then you would flood the LINK with status interrupts), and the LINK reads the PHY register field to find out the reason for the PHY_Interrupt, and resets the cause bits at its leisure.

I suggest deleting the comment.

(CWS8) Table 5-14 p48 and Table 5-13 p47 (T) If Bias is unfiltered, then the Bias_chnge bit needs to work on a filtered value of Bias, or else there is a danger of an interrupt flood. However, this might in turn confuse the LINK, which will see the interrupt, read a false zero on the Bias bit, and think there's no connection, but the real state is that Bias is detected and there will be no further interrupt to the LINK to alert it to this fact.

My conclusion is that Bias has to be filtered (this is the safest option and harmless). Add "The value reported by this bit shall be filtered by hysteresis logic to reduce multiple status changes caused by contact scrape when a connector is inserted or removed."

(CWS9) 5.2.1 p49 (E) final sentence - the Neg_Speed and Enab_Token are also not in the legacy map. Better to reword this sentence positively referring to Astat, Bstat, Ch and Con.

(CWS10) Clause 5.3 p50 (T) This is the subject of a separate contribution, already sent to the reflector.

(CWS11) Table 6-1 p53 (E) Now we have a defined set of PHY registers, the "derived from" column can be cleaned up to refer to them directly (already done for L)

(CWS12) Clause 6.1.2 P55 (T) We agreed last time on the timing of the physical LK-ON signal. This needs to be captured somehow, either in this clause or somewhere in Clause 5 with a two-way cross-reference to this Clause. I suggest the text:-

"A physical signal implementing the LINK_ON event shall be transmitted if the AND of LPS and the PHY register L bit is zero, and shall continue to be transmitted until the AND of LPS and the PHY register L bit becomes 1."

(CWS13) 6.1.5 p 57 (E/T) the ping timer needs describing somewhere, including its frequency, granularity and when it is reset! Also, the need for the PHY to process ping packets received from the local link needs to be described somewhere. (NB I understand that Intel may be bringing a proposal that the ping timer should be in the LINK).

(CWS14) Table 6-4 p57 (E) type has value 0 (in the "derived from" column)

(CWS15) Figure 6-6 p61 (T) the transition R1:R0 should have the action reset_time = RESET_TIME, so that you do always long reset (rather than repeat a short reset) after an arb_timer timeout (I believe this is in Bill Duckwall's document)

(CWS16) Table 6-8 (T) boolean reset_detected(): The value 85 ms needs to be given a name - is it RESET_DETECT (which is 85 microseconds, not 85 ms!)?

(CWS17) Table 6-11 p 75 line -9 and -8 (T/E): This refers to proxy_ID - but I believe we are not doing proxy pinging. The packet extended type = 1 cannot now occur, and so the two lines should be deleted.