PHY-Link Rules
Revision 0.2

History:
Revision 0.1: Presented at May 1394a Meeting.

Table 1: PHY / Link Behavior for LREQ Signalling

Link Behavior		Phy Behavior	
Request Type	**When LREQ Sent[1]**	**If Packet Arrives**	**If Status Transfer Starts**
Fair / Priority	After 1 Idle Clock	LREQ discarded, except when arb-acceleration is enabled, cycle-sync is not active, and an ACK packet is being received.	LREQ queued.
Immediate	After Packet Address Decode During Receive	CTL[0:1] may be in receive state since it is receiving the current packet, but a new packet cannot be seen at this time. LREQ queued.	LREQ queued
Isochronous	In iso period, data is ready to transmit, and CTL[0:1] are in receive or transmit states.	LREQ queued.	LREQ queued, unless subaction gap is seen, then LREQ canceled[2].
Register Read	Anytime	LREQ completed since interface is not required for register writes.	
Register Write	Anytime	LREQ queued[3].	
CycleSync	As soon as possible after the 125us counter rolls over, and the link is not the cycle master	PHY sets cycleSync flag. PHY clears cycleSync flag at first subaction gap.	

Notes:
1. Link always shifts out entire LREQ, even when arbitration is lost.
2. This is an error condition that should not occur, because the link must send LREQ during a current receive or transmit.
3. The link should not send multiple read requests to the PHY. The PHY will have indeterminate behavior if this is done. It may discard later requests, or discard earlier requets. The link should only send another read request after the PHY has completed the previous read by issuing a status transfer.

Remaining Questions:
1. If a link issues a priority request in between a transmit and a received ack, then determines it must issue a cycleSync LREQ, does the link wait for the priority request to be serviced, then send the Cycle Sync LREQ, or does it send the Cycle Sync LREQ immediately? If it sends the Cycle Sync LREQ immediately, does that cancel the priority request?
2. When a link sends an immediate request to send an acknowledge, then when the bus becomes idle (between the receive and the ack), can the link send a priority / fair LREQ? This is an enhanced aribtration question. I think it needs to do this, but the PHY needs to know not to cancel the immediate LREQ.