Link Power Status (LPS) Need

- Turns off PHY-LINK Interface when LINK is powered down
  - OFF
    - protects I/Os from excessive current
    - reduces PHY power consumption
    - PHY ignores unknown states of PHY-LINK inputs
  - ON
    - resets PHY-LINK interface when LINK is powered up

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LPS Reset

- PHY-LINK Interface Reset mechanism
  - power initialization
  - recover from “hung” PHY-LINK Interface
- can be used for:
  - host power reset
  - software initiated reset
- LPS well behaved
  - does not generate 1394 bus reset

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1394 LPS Proposal

- LPS communicates LINK power status
  - if LINK power is OFF, LPS = 0
  - if LINK power is ON, LPS = 1 or switching waveform
- LPS resets the PHY-LINK interface by signaling a power cycle sequence
- “switching waveform”
  - works in isolated environments

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1394 LPS Proposal - PHY

- PHY senses LPS active when:
  - LPS = 1 (immediately)
- PHY senses LPS inactive when:
  - LPS = 0 for more than 2.75us
- when PHY senses LPS inactive
  - all PHY-LINK outputs are driven to 0, including clk, control, Lreq, and data signals

1394 LPS Proposal - LINK Power Sensing

- LINK drives LPS active/switching when power is valid
- LPS inactive when power is not valid

1394 LPS Proposal - LINK RESET

- LINK drives LPS inactive for longer than 2.75us to reset the PHY-LINK interface
  - PHY drives clk to 0 when LPS is inactive
- LINK drives LPS active/switching to complete reset sequence
  - LINK drives control/data/Lreq to 0
  - LINK drives control/data to Z after receiving third rising PHY clk

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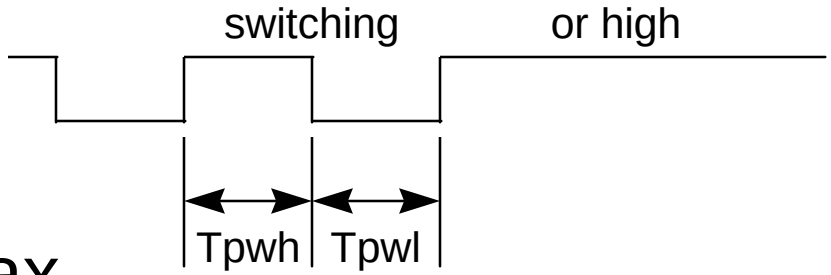
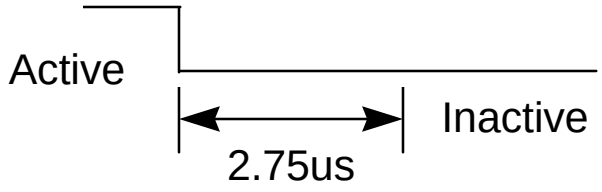
1394 LPS Proposal - Timing

- LPS active
  - Tpwh = 90ns min
  - Tpwl = 2.25us max
- LPS inactive
  - Tl = 2.75us min





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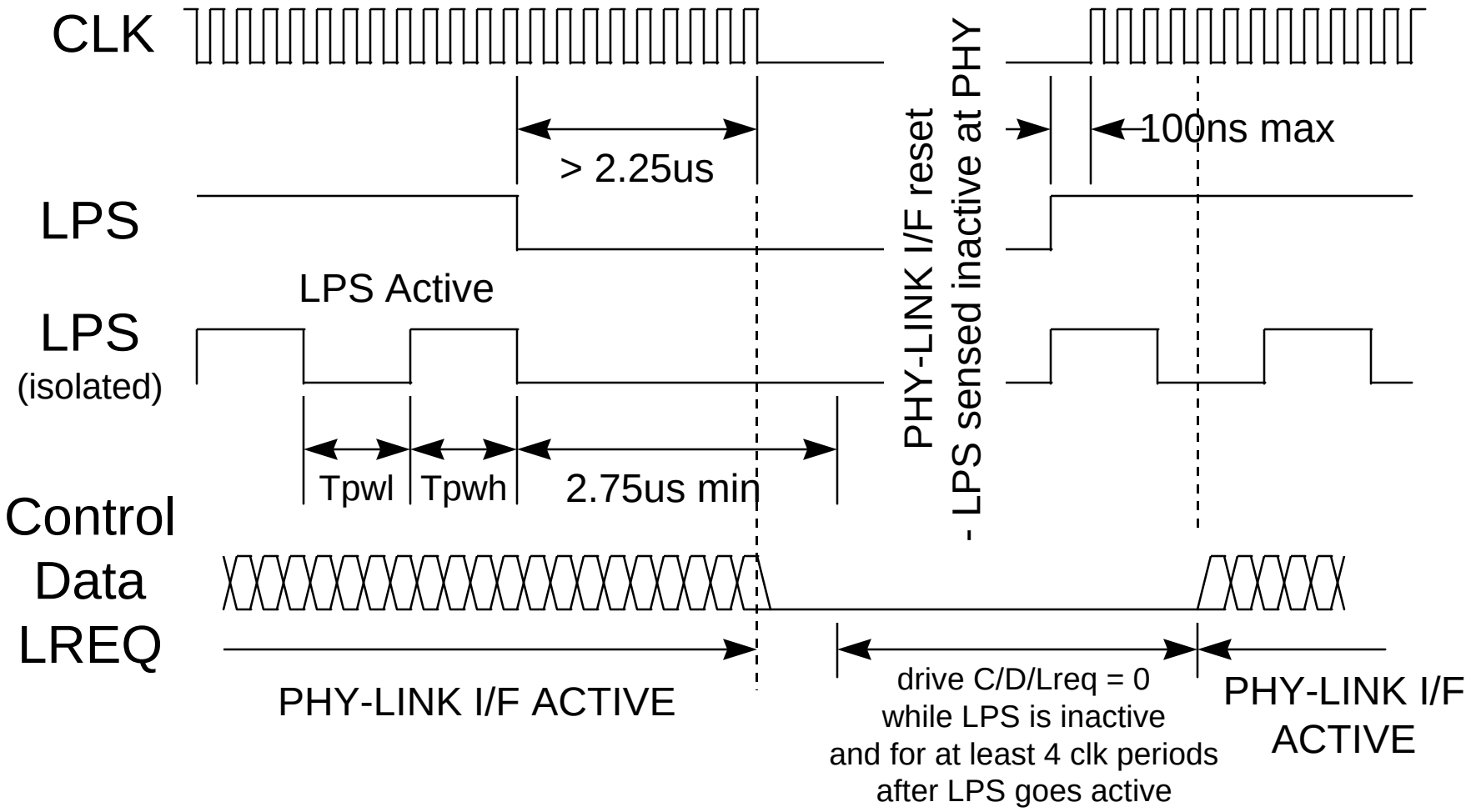
PHY-LINK LPS Timing reset (at PHY)



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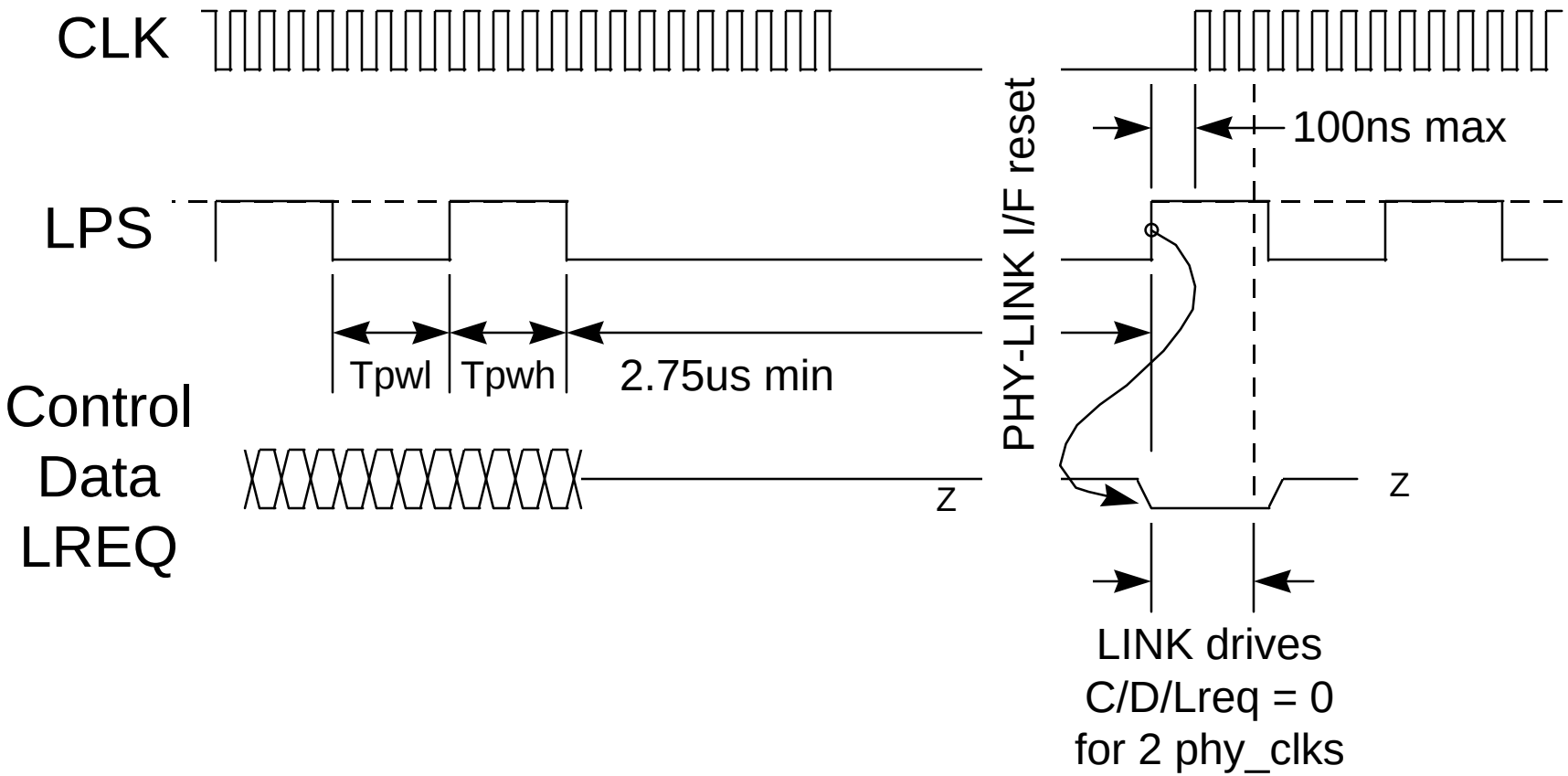
PHY-LINK LPS Timing reset (at LINK)



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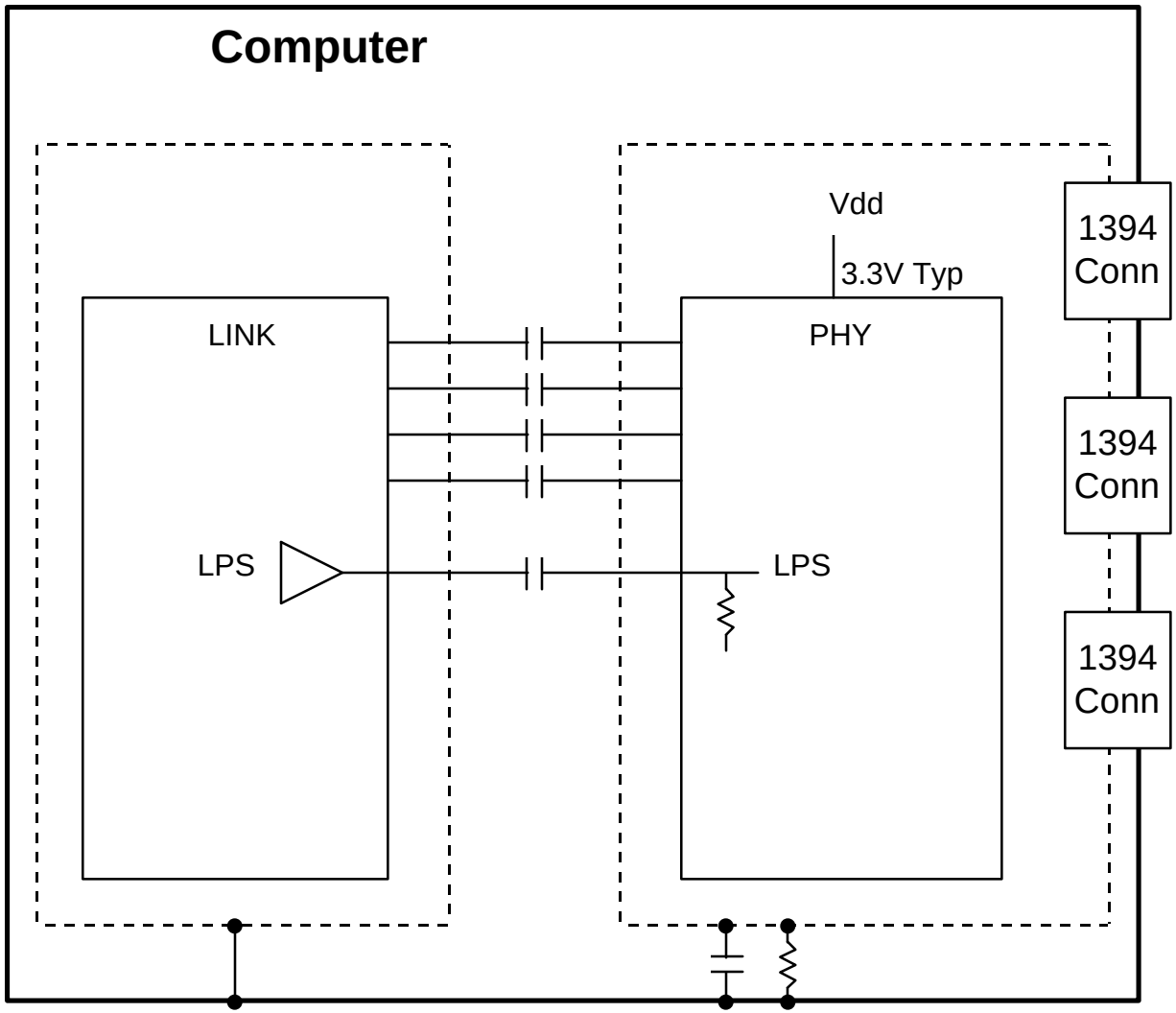
ISOLATED PHY-LINK Interface



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TEXAS

DIRECT PHY-LINK Interface