LREQ Issues

- What does “in isoch phase” mean for iso LREQ?
  - *Not only* receiving and transmitting isoch packets
  - Also includes receiving/sending CycleStart packet
    - **Link must send LREQ before entire CycleStart received**
- Proposal
  - State “in iso phase or during CycleStart reception...” for iso LREQ.
  - Add language that cycle start needs to be predicted.
    - **If not cycle start (ex. bad CRC), when granted, release bus.**

LREQ Issues

- Multi-speed Concatenation
  - When downshifting to S100, must issue another LReq
  - In links with multiple transmit data streams, may not be able to transmit LREQ while Xmitting current packet
    - **Packets concatenated into a transmit FIFO**
  - Can link use delay through PHY to its advantage?
    - **PHY is asserting data end for .24μs (12 SCLKs)**
    - **This occurs while PHY-LINK interface is IDLE**
- Propose change to LREQ Table for Isochronous
  - "...while CTL[0:1] is in receive or transmit and up to 10 SCLKs after last isochronous transmit."

LREQ Issues

- Background
  - Link has Xmitted priority request for enhanced arb
  - Did so while waiting for ack for previous transmit
  - Link determines it then must send Cycle Sync
    - **Does it wait for priority request to be serviced, or...?**
    - **Does it send Cycle Sync Immediately?**
      - **If yes, does that cancel the previous priority request?**
- Proposal
  - Link sends CycleSync LREQ
  - PHY does not cancel priority request

LREQ Issues

- Background
  - Link receives packet, sends LREQ for ack
  - How does it concatenate to its own ack?
    - **Does it send a priority/fair request?**
    - **If yes, PHY should not cancel immediate request**
- Proposal
  - Link sends priority/fair request
  - PHY does not cancel immediate request