Proposed change to P1394a Draft Revision 0.90, Section 6.1, page 58:

"If a node uses cable power, it shall meet the following requirements:

⇒ It shall consume no more than 3 Watts (as measured at the 1394 cable connection) for its PHY ~~1 W of power~~ after a power reset or after being initially connected to the bus (transition from all ports unconnected to any port connected). The receipt of a PHY link-on packet shall enable the node to consume additional power up to the limit specified by the node's self-ID packet(s);"

Nodes may be part of a module that implements a "soft" power switch. When the module connected to the electric mains is powered off, the preferred method to power the PHY is a trickle source from the electric mains. For battery powered modules that are powered off or for other modules when trickle power is not feasible, the preferred alternative is to power the PHY from the cable. The last alternative, an inactive PHY and a break in the bus power distribution, is permitted, however it is not a recommended implementation.

Proposed change to P1394a Draft Revision 0.90, Section 6.2.1, page 61, Table 6-2:

Table 6-2 — Self-ID packet fields (Continued)

Field	Derived from	Comment
pwr	POWER_CLASS	Power consumption and source characteristics: 000 Node does not need power and does not repeat power. 001 Node is self-powered and provides a minimum of 15 W to the bus. 010 Node is self-powered and provides a minimum of 30 W to the bus. 011 Node is self-powered and provides a minimum of 45 W to the bus. 100 Node may be powered from the bus (using up to 3 W for its PHY only); Node may be providing power to the bus[a]. 101 Node is powered from the bus and is using up to 3W. An additional 2 W is needed to enable the Link and higher layers[b]. 110 Node is powered from the bus and is using up to 3W. An additional 5 W is needed to enable the Link and higher layers[b]. 111 Node is powered from the bus and is using up to 3W. An additional 9 W is needed to enable the Link and higher layers[b].

[a.] The power providing capability of this node implementation is defined in ROM CSR space.
[b.] The link and higher layers are enabled by the link-on PHY packet described in clause 6.2.2 of IEEE Std 1394-1995.