No	Issue	Description	Status	Action
1	4-pin cable and connector	In Draft D0.09 - Open Issue: Has Enough information presented to retain consideration?	Open issue	
2	PHY/Link interface - PHY register map(s)	In Draft D0.09	Stable	
3	PHY/Link interface - PHY status reporting	In Draft D0.09 - Are all the corner cases covered? They've received wide attention in the meetings and on the reflector(s), but are they in the draft? Latest rule:- PHY should defer servicing a read register request from the link during a timing window (to be defined) before the detection of the subaction gap	Agreed, subject to confirmation	PK to provide text for rule and proposed timing
4	PHY/Link interface - LReq formats	In Draft D0.09	Stable	Draft to include requirement to support legacy 7-bit bus request LReq
5	PHY/Link interface - AC timing	In Draft D0.09	agreed, subject to no identified problems, minor typos	
6	PHY/Link interface - PHY-LINK handover	In Draft D0.09 - is an extra cycle required? Other changes in latest draft need confirmation. Question (from Hasegawa-san) that the link cannot insert MORE than one idle. Item for discussion	Open issues	
7	Cable PHY enhancements - "Caboose" packet	In Draft D0.09 - remove for legacy silicon reasons? Is mitigation for legacy reasons sufficient? How then to report speed?	Open issue	
8	Cable PHY enhancements - Ping packet	In Draft D0.09	Stable	
9	Cable PHY enhancements - ACK-accelerated arbitration	In Draft D0.09, Link PHY mechanism to be evaluated (see 10)	Agreed with open issue	
10	Cable PHY enhancements - Fly-by arbitration	In Draft D0.09 Issue: Link-PHY: how is this indicated by the link? (concatenated packet scenario)	Agreed with open issue	
11	Cable PHY enhancements - Multi-speed packet concatenation	In Draft D0.09	Stable	
12	Cable PHY enhancements - Per port disable	In Draft D0.09 Issue: PHY mechanism for link control? The relationship between suspend / resume and per port disable needs to be sorted out. (slightly different twists of fundamentally the same mechanism?). The discussion that resolves how they are alike and how they differ should flush out the remaining details.	Open issue	

No	Issue	Description	Status	Action
13	Isochronous connection management	In Draft D0.09 Issue: higher speeds require specification?	Needs careful review	
14	Clarifications and corrigenda - Acknowledge codes (ack_tardy)	In Draft D0.09	Stable	
15	Clarifications and corrigenda - Response code usage	In Draft D0.09	Stable	
16	Clarifications and corrigenda - Quadlet vs. block read and write requests	In Draft D0.09	Stable	
17	Clarifications and corrigenda - Command reset effects	In Draft D0.09	Stable	
18	Clarifications and corrigenda - Unit registers (reserved address spaces)	In Draft D0.09	Stable	
19	Clarifications and corrigenda - ROM Bus_Info_Block	In Draft D0.09 Link speed and other items	Stable	
20	Clarifications and corrigenda - Determination of the bus manager	In Draft D0.09	Stable	
21	Clarifications and corrigenda - Automatic activation of the cycle master	In Draft D0.09	Stable	
22	Clarifications and corrigenda - Cycle too long error	In Draft D0.09	Stable	
23	Clarifications and corrigenda - Abdication by the bus manager	In Draft D0.09	Stable	
24	Clarifications and corrigenda - Security extensions	In Draft D0.09 - language needs tightening up to be acceptable to legal beagles?	Stable, subject to legal opinion	MB to procure a legal review

No	Issue	Description	Status	Action
25	More than 63 nodes	PHY modifications for graceful degradation when more than 63 nodes are present. How is physical ID 0x3E supposed to be guaranteed set aside so that the root can claim it?	Agreed in principle, implementn open issues	State machine modifications
26	Priority requests for response packet transmission	Proposal:- any node be permitted to send ONE response packet without regard for fairness, that this response packet not be counted against the node's fair arbitration and that additional response packets be sent according to fair arbitration rules (i.e., they can compete with outbound request packets for whatever fair arbitration opportunities are permitted by the rules).	Agreed in principle - is this rule OK?	
27	Bus_Info_Block - bootable device	Bit to indicate "bootable" device. Better solved in the new IEEE 1212?	open issue	
28	Bus_Info_Block - generation bit	In Draft D0.09 - "Generation" bit - new text in clause 9.7	agreed subject to confirmation	
29	Bus_Info_Block - max_rec	max_rec to indicate maximum for both read and write?	open issue requires agreement	
30	Length of arbitrated short reset	Variability of length of arbitrated (short) reset signal (long distance PHY and cable issue). NB There's a related issue, about root contention timings (does this need a separate place holder in this issues summary.)	Requirement agreed, solution an open issue	
31	Sleep mode (a.k.a. suspend / resume)	Method for Link to instruct PHY to put a port to sleep; method for a pair of ports to synchronise going to sleep, method for remotely initiated sleep to be reported by PHY to link, method for port to maintian connection status during sleep, method for Link to put PHY to sleep, method for link to wake up PHY, method for link to wake up port, method for port pair to wake up, method for remotely initiated wake up to be reported.	overall requirement agreed	
32	PHY/Link reset	Method to reset PHY/Link interface - rely on state-machine timeouts, use LPS low, new LREQ or new reg bit???	agreed in principle to rely on timeout, possibly also use LPS	RB to propose text
33	Dual-phase retry		agreed	verify state machines for correctness
34	Power distribution, agencies	Agency compliance (safety) issues. DWs summary (very brief) is in 97-203r0 on the FTP site.	Power rangers propose Informative Annex	SB and JB to provide the needed drawings and text---whether normative or informative---
35	Power distribution, voltages	New clause 6.1 in Draft D0.09 - major revision following recommendations from Power Rangers	Clause 6.1 requires confirmation	
36	Speed signal sampling requirements	tighter specification required for speed signal in order to ensure interoperability	Agreed in principle	JS to propose text

No	Issue	Description	Status	Action
37	How to set the gap count	??	open?	
38	Formal definition of an ACK packet for the PHY	??	open	
39	Recommended interval between software-initiated bus reset(s)		open	
40	Extended speed codes for SPEED_MAP		Agreed in principle	PJ to propose text
41	"Fairness" optimizations	two proposals for methods for allocating a node multile accesses per fairness interval	open issue	
42	Electrical isolation / Annex A	In Draft D0.09, Was there more useful information in Annex A 1394-1995 that is worth salvaging? Need someone with the expertise to salvage any of it.	agreed in principle, more work on text and subject to review	
43	Asynchronous streams (tcode 0x0A)	In Draft D0.09 - New Clause 7	agreed, subject to confirmation	
44	PHY/Link interface DC timing	As in Draft D0.09	agreed, subject to review	
45	Availability of SClk	Should Sclk be available when all ports are disabled? This issue subsumed within the overall power rangers requests?	open issue	
46	LReq summary table	In Draft D0.09. Issue concerning interaction between cycle sync and priority request, issue concerning when priority and fair requests may be sent after immediate requests, issue concerning which requests to use for ACK-accelerated arbitration (packet concatenation), issue concerning over-restricted spec for isoch packets	partly agreed, but with open issues	
47	PHY/Link interface signals	Draft D0.09. LPS: optional on link, required on PHY LinkOn: optional on link, required on PHY Direct: optional on link, required on PHY	Agreed, subject to confirmation	
48	Location of the ping timer	Should the ping timer be in the PHY or in the link. Need to ensure sufficient accuracy (to appropriate resolution)	open issue	JH to provide recommendation
49	Cable line state	In Draft D0.09 - new RX_TOKEN_GRANT	agreed	
50	Read response for data block	In Draft D0.09 - new text	agreed, subject to confirmation	
51	Token-style Arbitration	Allows optimisation of isochronous transfers in a sub-tree - As described in Bill Duckwall's 1394 optimisations document	agrreed in principle	PJ to provide text and state machine modifications
52	Max Bus Hold	Clarify that MAX_BUS_HOLD is guaranteed by the Link, not by the PHY.	agreed in principle	PJ to add text to draft