IEEE P1394a
SCAT - Scope and Closing Actions Table - 1 August, 1997

2	PHY/Link interface - PHY register map(s)	In Draft D0.09	Stable	
4	PHY/Link interface - LReq formats	In Draft D0.09	Stable	Draft to include requirement to support legacy 7-bit bus request LReq
8	Cable PHY enhancements - Ping packet	In Draft D0.09	Stable	
14	Clarifications and corrigenda - Acknowledge codes (ack_tardy)	In Draft D0.09	Stable	
15	Clarifications and corrigenda - Response code usage	In Draft D0.09	Stable	
16	Clarifications and corrigenda - Quadlet vs. block read and write requests	In Draft D0.09	Stable	
17	Clarifications and corrigenda - Command reset effects	In Draft D0.09	Stable	
18	Clarifications and corrigenda - Unit registers (reserved address spaces)	In Draft D0.09	Stable	
19	Clarifications and corrigenda - ROM Bus_Info_Block	In Draft D0.09 Link speed and other items	Stable	
20	Clarifications and corrigenda - Determination of the bus manager	In Draft D0.09	Stable	
21	Clarifications and corrigenda - Automatic activation of the cycle master	In Draft D0.09	Stable	
22	Clarifications and corrigenda - Cycle too long error	In Draft D0.09	Stable	

23	Clarifications and corrigenda - Abdication by the bus manager	In Draft D0.09	Stable	

5	PHY/Link interface - AC timing	In Draft D0.09 (no objections raised 25 Jun 97)	Agreed	Minor typos
7	Cable PHY enhancements - "Caboose" packet	In Draft D0.09, vote to extend scope to include Power Class in caboose packet 25 Jun 97	Agreed	PJ to propose Power Class information caboose packet description in next draft, (NB may be superseded by proposal from Power Managers)
9	Cable PHY enhancements - ACK-accelerated arbitration	In Draft D0.09, but see 46	Agreed	
10	Cable PHY enhancements - Fly-by arbitration	In Draft D0.09, but see 46	Agreed	
28	Bus_Info_Block - generation bit	In Draft D0.09 - "Generation" bit - new text in clause 9.7, agreed 25 jun 97	agreed	
29	Bus_Info_Block - max_rec	max_rec to indicate maximum for both read and write. agreed 25 Jun 97	agreed	
42	Electrical isolation / Annex A	In Draft D0.09 - New Annex A agreed 24 Jun 97	Agreed	
43	Asynchronous streams (tcode 0x0A)	In Draft D0.09 - New Clause 7 agreed 24 jun 97	Agreed	
44	PHY/Link interface DC specification	In Draft D0.09 agreed, as no objections raised 25 Jun 97	agreed	
47	PHY/Link interface signals	Draft D0.09. LPS: optional on link, required on PHY LinkOn: optional on link, required on PHY Direct: optional on link, required on PHY - agreed 24 Jun 97	Agreed	
48	Ping timer	In the Link - agreed 24 jun 97	Agreed	
49	Cable line state	In Draft D0.09 - new RX_TOKEN_GRANT	Agreed	
50	Read response for data block	In Draft D0.09 - new text - agreed 24 Jun 97	Agreed	
57	LPS AC specification	As per presentation by RB/NM on 24 Jun 97	Agreed	PJ to include in next draft
64	SPEED_SIGNAL_LENGTH vs SPEED-SIGNAL-TIME	two terms for the same value?	Agreed	PJ to verify and add correction
66	BANDWIDTH_AVAIL > S400	If 8.1.2 survives, then calculations in the paragraph on the overhead field need updating (spd and/or xspd)	Agreed	PJ to make appropriate modification if necessary

24	Clarifications and corrigenda - Security extensions	In Draft D0.09 - language needs tightening up to be acceptable to legal beagles?	Agreed in principle	MB to procure a legal review
26	Priority requests for response packet transmission	Proposal:- any node be permitted to send ONE response packet without regard for fairness, that this response packet not be counted against the node's fair arbitration and that additional response packets be sent according to fair arbitration rules (i.e., they can compete with outbound request packets for whatever fair arbitration opportunities are permitted by the rules).	Agreed in principle	general review of rule for final confirmation
33	Dual-phase retry		agreed in principle	PJ to verify state machines for correctness, and prepare clarification text
36	Speed signal sampling requirements	tighter specification required for speed signal in order to ensure interoperability	Agreed in principle	JS to propose text
51	Token-style Arbitration	Allows optimisation of isochronous transfers in a sub-tree - As described in Bill Duckwall's 1394 optimisations document. NB support for Token Style arbitration should be optional (decided 24 Jun 97)	Agreed in principle	PJ to provide text and state machine modifications
52	Max Bus Hold	Clarify that MAX_BUS_HOLD is guaranteed by the Link, not by the PHY.	Agreed in principle	PJ to add text to draft
53	PHY behaviour on LPS -> 0	When LPS -> 0 (for longer than 2.4 usec), PHY takes SClk, CTL and DTA to zero.	Agreed in principle	RB to provide PJ with text for inclusion in next draft
55	Ping timer mechanism	Overall description of use of ping timer, JH working on evaluating the trade-offs of detailed options	Agreed in principle	JH to provide text for inclusion in next draft
56	Connector and cable testing	Templates for cable and connector tests, as presented on 24 Jun 97	Agreed in principle	EH to provide templates and text to PJ for inclusion in next draft
58	Isoch LReq	Need tighter defn of "in isoch phase", as JB presented on 24 Jun 97	Agreed in principle	JB to revise Lreq table
59	Lreq for multi-speed concat	Links may not be able to transmit Lreq whilst transmitting another packet - propose to allow Iso Lreq up to 10 Sclks after last iso transmit	Agreed in principle	JB to revise Lreq table
60	Cycle sync after pri req for enhanced arb	Does the link wait for pri req to be service or send Cycle sync immediately - propose the latter, and PHY does not cancel priority request	Agreed in principle	JB to revise Lreq table
63	Power-on (hard) reset states for PHY registers	All PHY registers to have defined "power-on/hard reset" states	Agreed in principle	PJ to include in next draft

69	enab_accel	Revised behaviour - using PHY learning, as per Ganesh Murthy proposal on 24 Jun	Agreed in principle	GM to provide text to PJ for incorporation into next draft
70	Link to check CYCLE_START	Link should look at whole of first quadlet, not just the TCode, for cycle start, in order to provide greater robustness	Agreed in principle	PJ to prepare wording for review

1	4-pin cable and connector	In Draft D0.09 - Open Issue: Concern on emissions etc. (and concern on grounding)	Open issue	Further information to be presented in August meeting, Kenji Keino to send Sony presentation of 24 Jun 97 to PJ to be put on ftp site, with Japanese translated into English
3	PHY/Link interface - PHY status reporting	In Draft D0.09 - Are all the corner cases covered? They've received wide attention in the meetings and on the reflector(s), but are they in the draft? Latest rule:- PHY should defer servicing a read register request from the link during a timing window (to be defined) before the detection of the subaction gap	Agreed, subject to confirmation	PK to provide text for rule and proposed timing to PJ for inclusion in next draft
6	PHY/Link interface - PHY-LINK handover	In Draft D0.09 - is an extra cycle required? Other changes in latest draft need confirmation. Question (from Hasegawa-san) that the link cannot insert MORE than one idle. Item for discussion. Presentation from Sean Killeen.	Open issues	Review spec and SK presentation on reflector
12	Cable PHY enhancements - Per port disable	In Draft D0.09 Issue: PHY mechanism for link control? The relationship between suspend / resume and per port disable needs to be sorted out. (slightly different twists of fundamentally the same mechanism?). The discussion that resolves how they are alike and how they differ should flush out the remaining details.	Open issue	Task group to propose suspend/resume mechanisms by Jul 24
13	Isochronous connection management	In Draft D0.09 Propose to limit this to definition of register locations only, with informative cross-reference to IEC 1883 - to be confirmed in August	Open issue	confirm proposal to reduce this clause in August meeting, editors note to this effect in the next draft
25	More than 63 nodes	PHY modifications for graceful degradation when more than 63 nodes are present. How is physical ID 0x3E supposed to be guaranteed set aside so that the root can claim it?	Open issue, general principle agreed	State machine modifications required - not clear who has the action
27	Bus_Info_Block - bootable device	Bit to indicate "bootable" device. Better solved in the new IEEE 1212?	open issue	
30	Length of arbitrated short reset	Variability of length of arbitrated (short) reset signal (long distance PHY and cable issue). NB There's a related issue, about root contention timings (does this need a separate place holder in this issues summary.)	Requirement agreed, solution an open issue	

31	Sleep mode (a.k.a. suspend / resume)	Method for Link to instruct PHY to put a port to sleep; method for remote node to put a port to sleep; method to wait until a remote port has been put to sleep; method for port to maintian connection status during sleep, method for Link to put PHY to sleep, method for link to wake up PHY, method for link to wake up port, method for port pair to wake up, method for remotely initiated wake up to be reported. See also 45	overall requirement agreed	CC/SB to lead a task group to firm up requirements and propose mechanisms (publicise by Thursday 24th July)
32	PHY/Link reset	Method to reset PHY/Link interface - rely on state-machine timeouts, use LPS low, new LREQ or new reg bit??? See also Nos 53 and 54.	agreed in principle to rely on timeout, suspend further consideration of using LPS (only reconsider if timeout is not practical)	JB/JH to prepare proposal for state machine timeouts (or confirm that current mechanisms are adequate)
34	Power distribution, agencies	Agency compliance (safety) issues. DWs summary (very brief) is in 97-203r0 on the FTP site.	Power rangers propose Informative Annex	SB and JB to provide the needed drawings and text---whether normative or informative---
35	Power distribution, voltages	New clause 6.1 in Draft D0.09 - major revision following recommendations from Power Rangers	Current text agreed as far as it goes, more text anticipated	Power Rangers to provide further text by 24th July
37	How to set the gap count	Specified in Draft D0.09	agreed subject to confirmation	review for final confirmation
38	Formal definition of an ACK packet for the PHY	Any 8-bit packet	proposed 15Jul97	
39	Recommended interval between software-initiated bus reset(s)		open issue	PJ to ensure someone has the action to make a proposal
40	Extended speed codes for SPEED_MAP	In Draft D0.09	Agreed subject to confirmation	
41	"Fairness" optimizations	As described in 97-015r2 and presented on 24 Jun 97 Reset values:- Disks, PC's and bridges allowed to default pri_req to pri_ref	Agreed with minor modifications and subject to confirmation	DLaF to send details of modifications to PJ, PJ to include in the next draft
45	Availability of SClk	Should Sclk be available when all ports are disabled? See also 31	open issue	To be resolved by Sleep mode Task Force
46	LReq summary table	In Draft D0.09.Issues split out - See 58, 59 60. Speed checking proposal:- Whoever does the concatenation checks the speed. At most one arbitration per LReq.	Proposed 14Jul97	JB to provide revised table

54	Link initialisation of PHY-Link Interface	Possible problem when using an isolation barrier, requiring C/D/LReq to be taken to zero for two cycles when Sclk is seen	Open issue	RB/NM to describe problem on reflector, then YH to describe his (informative) solution
61	Root contention timings	With longer cables, there may be timing problems with ROOT_CONTEND_FAST and ROOT_CONTEND_SLOW times, we may need to changes these timings, and there's interopability with legacy PHYs.)	Open	Dave LaFollette to prepare proposal
62	PHY version registers	As proposed by JF - agreed to extend scope to accept such a proposal	proposal for review	PJ to include proposal in next draft with editor's note to say that the proposal is subject to review
63	P1394/P1394a interoperability	Is all reasonably desired interoperability supported?	Open	All WG members to review and comment
65	Lock transactions	Issue with future compatibility when performing lock transactions on registers with reserved fields	Open issue	PY to discuss with Dave James and report results on the reflector
67	Asynch packets at CYCLE_START time	Link will restrain from sending asynch packets at round about cycle start time, plus the current cycle synch mechanism	Proposed 14jul97	
68	FORCE_ROOT_TIMEOUT	Max value is too large (two long daisychains with either end contending for root)	Open	Dave LaFollette to propose new value