IEEE P1394a
SCAT - Scope and Closing Actions Table - 6 August, 1997

1	4-pin cable and connector	In Draft D0.09 - Open Issue: Concern on emissions etc. (and concern on grounding)	Open issue. Motion to delete Clause 4 tabled until September meeting	Further information to be presented in September meeting, Kenji Keino to send Sony presentation of 24 Jun 97 to PJ to be put on ftp site, with Japanese translated into English
7	Cable PHY enhancements - "Caboose" packet	In Draft D0.09, vote to extend scope to include Power Class in caboose packet 25 Jun 97, action on PJ to propose Power Class information caboose packet description in next draft put on hold, pending discussions on power management	Agreed in principle, but may be re-opened	
12	Cable PHY enhancements - Per port disable	In Draft D0.09 Issue: PHY mechanism for link control? The relationship between suspend / resume and per port disable needs to be sorted out. (slightly different twists of fundamentally the same mechanism?). The discussion that resolves how they are alike and how they differ should flush out the remaining details. Proposal on the table. See 31	Open issue, proposal on the table	See 31
26	Priority requests for response packet transmission	Proposal:- any node be permitted to send ONE response packet without regard for fairness, that this response packet not be counted against the node's fair arbitration and that additional response packets be sent according to fair arbitration rules (i.e., they can compete with outbound request packets for whatever fair arbitration opportunities are permitted by the rules). Unfinished discussion on 5 Aug 97 re-opened the issue	Open issue	general review of rule for final confirmation
31	Sleep mode (a.k.a. suspend / resume)	Method for Link to instruct PHY to put a port to sleep; method for remote node to put a port to sleep; method to wait until a remote port has been put to sleep; method for port to maintian connection status during sleep, method for Link to put PHY to sleep, method for link to wake up PHY, method for link to wake up port, method for port pair to wake up, method for remotely initiated wake up to be reported. Proposal on the table. See also 45	overall requirement agreed, proposal on the table	all to review suspend resume proposal
45	Availability of SClk	Should Sclk be available when all ports are disabled? See also 31	open issue, proposal on the table	see 31
54	Link initialisation of PHY-Link Interface	Possible problem when using an isolation barrier, requiring C/D/LReq to be taken to zero for two cycles when Sclk is seen	Agreed subject to confirmation	see 57

57	LPS specification	LPS means “give me SClk”. LPS AC specification agreed as per presentation by RB/NM on 24 Jun 97. Link can reset PHY-Link interface by taking LPS low (see 32). See 53. See 54.	Agreed subject to confirmation	RB to provide PJ with text
63	P1394/P1394a interoperability	Is all reasonably desired interoperability supported?	Open	All WG members to review and comment
68	FORCE_ROOT_TIMEOUT	Max value is too large (two long daisychains with either end contending for root)	Open	PHY designers to review and provide new value
74	Electrical specifiation for S400 serial transmission	Min rise time of 500 ns required, sensitivity of, say, 60 mV rather than current spec of 112 required in order to provide sufficient margin	In scope for next meeting	EH to provide proposed modification for confirmation at next meeting

3	PHY/Link interface - PHY status reporting	PHY should defer servicing a read register request from the link during a timing window (to be defined) before the detection of the subaction gap	Agreed in principle	PK to provide text for rule and proposed timing to PJ for inclusion in next draft
24	Clarifications and corrigenda - Security extensions	In Draft D0.09 - language needs tightening up to be acceptable to legal beagles?	Agreed in principle	All to solicit further legal review
30	Length of arbitrated short reset	Length of arbitrated (short) reset signal for long distance PHY and cable issue should be adjusted if necessary	Agreed in principle	PHY designers meeting to double check whether the value needs to be adjusted, and adjust accordingly
33	Dual-phase retry		agreed in principle	PJ to verify state machines for correctness, and prepare clarification text
36	Speed signal sampling requirements	tighter specification required for speed signal in order to ensure interoperability	Agreed in principle	JS to propose text
51	Token-style Arbitration	Allows optimisation of isochronous transfers in a sub-tree - As described in Bill Duckwall’s 1394 optimisations document. NB support for Token Style arbitration should be optional (decided 24 Jun 97)	Agreed in principle	PJ to provide text and state machine modifications
52	Max Bus Hold	Clarify that MAX_BUS_HOLD is guaranteed by the Link, not by the PHY.	Agreed in principle	PJ to add text to draft
55	Ping timer mechanism	Overall description of use of ping timer, JH working on evaluating the trade-offs of detailed options	Agreed in principle	JH to provide text for inclusion in next draft
56	Connector and cable testing	Templates for cable and connector tests, as presented on 24 Jun 97	Agreed in principle	EH to provide templates and text to PJ for inclusion in next draft
61	Root contention timings	Change ROOT_CONTEND_FAST and ROOT_CONTEND_SLOW times to deal with longer P1394a cables.. Agreed that 1394a will be modified accordingly	Agreed in principle	PHY designers review to finalise the revised constants

63	Power-on (hard) reset states for PHY registers	All PHY registers to have defined “power-on/hard reset” states	Agreed in principle	PJ to include in next draft
69	enab_accel	Revised behaviour - using PHY learning, as per Ganesh Murthy proposal on 24 Jun	Agreed in principle	GM to provide text to PJ for incorporation into next draft
70	Link to check CYCLE_START	Link should look at whole of first quadlet, not just the TCode, for cycle start, in order to provide greater robustness	Agreed in principle	PJ to prepare wording for review
72	gap_count calculation constants when using ping timing	various new constants are required for ping-timer-based gap count calculations - arb_response_delay, link_to_bus_delay, phy_delay (min value), bus_to_link_delay, ping_response_time will be defined as constants, and phy_delay_jitter will be reported	Agreed in principle	PHY designers review to verify constants, and to provide precise definition as to what each constant means

25	More than 63 nodes	Action on more than 63 nodes. PHY: don’t wrap beyond Node_ID of 63; :ink treat reception of a Self-ID packet with a Node_ID of 63 as a bus configuration error. Agreed 4 Aug	Agreed	PJ to insert text, PHY designers review to verify state machine
32	PHY/Link reset	Link can reset PHY/Link interface by using LPS low. See also Nos 53, 54 and 57	Agreed	See 57
34	Power distribution, agencies	Agency compliance (safety) issues. DWs summary (very brief) is in 97-203r0 on the FTP site. Informative Annex. Text from JB sent to PJ	Agreed	PJ to incorporate into next draft
35	Power distribution, voltages	New clause 6.1 in Draft D0.09 - major revision following recommendations from Power Rangers. 3W allowed “default” power consumption from a cable for a PHY	Agreed	PJ, SB and DW to prepare modified proposed text as discussed and PJ to incorporate into next draft
39	Recommended interval between software-initiated bus reset(s)	Software “should” wait at least 2 seconds	Agreed	JF to recommend text
41	"Fairness" optimizations	As per draft D0.9X, with modifications:- Field size is 6 bits (both fields byte aligned); Behaviour is undefined when PRI-REQ is written with a value larger than PRI_PREF.	Agreed	PJ to amend next draft
46	LReq summary table	In Draft D0.09.Issues split out - See 58, 59 60. Speed checking proposal:- Whoever does the concatenation checks the speed. At most one arbitration per LReq. Agreed 4 Aug. Don’t include any text which prohibits a PHY from checking a concatenated LReq and performing two arbitrations (thought compliant Links will never generate this)	Agreed	PJ to incorporate revised clarification text into next draft (with editorial amendments) CWS/PJ to prepare text on amplified speed rule for inclusion in next draft
53	PHY behaviour on LPS -> 0	When LPS -> 0 (for longer than 2.75 usec), PHY takes SClk, CTL and DTA to zero.	Agreed	see 57
58	Isoch LReq	Need tighter defn of “in isoch phase”, as JB presented on 24 Jun 97	Agreed	see 46

59	Lreq for multi-speed concat	Links may not be able to transmit Lreq whilst transmitting another packet - propose to allow Iso Lreq up to 10 Sclks after last iso transmit	Agreed	see 46
60	Cycle sync after pri req for enhanced arb	Does the link wait for pri req to be serviced or send Cycle sync immediately - agreed the latter, and PHY does not cancel priority request	Agreed	see 46
62	PHY version registers	As proposed by JF	Agreed	PJ to include proposal in next draft
64	SPEED_SIGNAL_LENGTH vs SPEED-SIGNAL-TIME	two terms for the same value?	Agreed	PJ to correct
66	BANDWIDTH_AVAIL > S400	If 8.1.2 survives, then calculations in the paragraph on the overhead field need updating (spd and/or xspd)	Agreed	PJ to make appropriate modification if necessary
71	Cycle Start starvation	Replace Cycle Sync LReq with two LReqs - Accelerate/Deaccelerate. Default state is Accelerate (but this only applies of enab-accel is also set). Agreed 4 Aug	Agreed	PJ to update draft
73	reserved for IEEE purposes	reserved fields should not be considered fair game by other standards or trade association bodies	Agreed	PJ to include statement that reserved means reserved for future IEEE definition
75	SClk specification	Specify as frequency +- 100ppm, plus 40% 60% duty cycle	Agreed	PJ to update in next draft
76	Annex C	Annex C is made informative in order to remove suggestion of isolation need for power pass-through	Agreed	PJ to update in next draft
77	PHY legacy register map	Not appropriate to incorporate this into P1394b	Agreed	PJ to remove and make appropriate other editorial adjustment in the next draft

2	PHY/Link interface - PHY register map(s)	In Draft D0.09	Stable	
4	PHY/Link interface - LReq formats	In Draft D0.09	Stable	
5	PHY/Link interface - AC timing	In Draft D0.09 (no objections raised 25 Jun 97)	Stable	
6	PHY/Link interface - PHY-LINK handover	Text in Draft (9X) confirmed 4 Aug - addition of a note on possibly backwards compatibility when using a link which does insert the extra IDLE	Stable	PJ to add note to next draft
8	Cable PHY enhancements - Ping packet	In Draft D0.09	Stable	
9	Cable PHY enhancements - ACK-accelerated arbitration	In Draft D0.09, but see 46	Stable	

10	Cable PHY enhancements - Fly-by arbitration	In Draft D0.09, but see 46	Stable	
11	Cable PHY enhancements - Multi-speed packet concatenation	In Draft D0.09, but see 46	Stable	
13	Isochronous connection management	Clause 9 to be removed- proposed June 24, voted Aug 4th	Stable	
14	Clarifications and corrigenda - Acknowledge codes (ack_tardy)	In Draft D0.09	Stable	
15	Clarifications and corrigenda - Response code usage	In Draft D0.09	Stable	
16	Clarifications and corrigenda - Quadlet vs. block read and write requests	In Draft D0.09	Stable	
17	Clarifications and corrigenda - Command reset effects	In Draft D0.09	Stable	
18	Clarifications and corrigenda - Unit registers (reserved address spaces)	In Draft D0.09	Stable	
19	Clarifications and corrigenda - ROM Bus_Info_Block	In Draft D0.09 Link speed and other items	Stable	
20	Clarifications and corrigenda - Determination of the bus manager	In Draft D0.09	Stable	
21	Clarifications and corrigenda - Automatic activation of the cycle master	In Draft D0.09	Stable	
22	Clarifications and corrigenda - Cycle too long error	In Draft D0.09	Stable	
23	Clarifications and corrigenda - Abdication by the bus manager	In Draft D0.09	Stable	

27	Bus_Info_Block - bootable device	Bit to indicate "bootable" device. Agreed that this is better solved in the new IEEE 1212 - 4 Aug	Stable	
28	Bus_Info_Block - generation bit	In Draft D0.09 - "Generation" bit - new text in clause 9.7, agreed 25 jun 97	Stable	
29	Bus_Info_Block - max_rec	max_rec to indicate maximum for both read and write. agreed 25 Jun 97	Stable	
37	How to set the local PHY's gap count	Specified in Draft D0.09	Stable	
38	Formal definition of an ACK packet for arbitration purposes in the PHY	Any 8-bit packet	Stable	
40	Extended speed codes for SPEED_MAP	In Draft D0.09	Stable	
42	Electrical isolation / Annex A	In Draft D0.09 - New Annex A agreed 24 Jun 97. Reconfirmed as normative on 5 Aug 97 (in order to replace the 1394-1995 normative annex)	Stable	
43	Asynchronous streams (tcode 0x0A)	In Draft D0.09 - New Clause 7 agreed 24 jun 97	Stable	
44	PHY/Link interface DC specification	In Draft D0.09 agreed, as no objections raised 25 Jun 97	Stable	
47	PHY/Link interface signals	Draft D0.09. LPS: optional on link, required on PHY LinkOn: optional on link, required on PHY Direct: optional on link, required on PHY - agreed 24 Jun 97	Stable	
48	Ping timer	In the Link - agreed 24 jun 97	Stable	
49	Cable line state	In Draft D0.09 - new RX_TOKEN_GRANT	Stable	
50	Read response for data block	In Draft D0.09 - new text - agreed 24 Jun 97	Stable	
65	Lock transactions	Draft 0.9X has new text to deal with issue with future compatibility when performing lock transactions on registers with reserved fields	Stable	
67	Asynch packets at CYCLE_START time	Issue removed by use of new Accelerate/Deaccelerate LReq (see No	Stable	