IEEE P1394a
SCAT - Scope and Closing Actions Table - 97-035r5 - 28 September, 1997

33	Dual-phase retry	State machines have inadequacies - how have implementations (if any) iinterpreted them?	Open	PJ to solicit input from implementers on the reflector,, and then to prepare clarification text
56	Connector and cable testing	Templates for cable and connector tests, as presented on 24 Jun 97, Annex K needs review	Open	Dave Brunker to propose modifications to Annex K
63	P1394/P1394a interoperability	Is all reasonably desired interoperability supported?	Open	All WG members to review and comment
76	Annex C	Proposed that Annex C is made informative in order to remove suggestion of isolation need for power pass-through	Open	DW to provide a proposal.
78	Mandatory vs Optional features	Need to review on what is mandatory, what is optional.for the link, for the PHY, etc	Open	All to review the current draft
79	Tree-ID	Proposal to make Tree-ID independent of cable length, 26 Sep 97	Open	All to review proposal
82	LinkOn specification	Currently poorly specified. CWS made a proposal to PHY designers. Further inadequacies exposed	Open	Joe Bennett to make a proposal on the spec and use of LinkOn
83	TOTAL_DATA_PREFIX	Need for this new constant agreed on 26 Sep 97. Straw polls favour 180 ns for S100, 120 (or 140) for higher speeds.Value to be decided at the next meeting.	Open	All to consider appropriate value(s)
85	Physical Configuration Limits	An Annex seems to be required on how to manage the topology of the bus.	Open	PJ will document in P1394A what we already know and which is not stated in -1995, A group will figure out what additional information needs to be added to the standard.

1	4-pin cable and connector	Agreed 25 Sep 97, with modified cable construction as presented in 97-060r0	Agreed in principle	Cable working group to provide newdrawings,
3	PHY/Link interface - PHY status reporting	PHY should defer servicing a read register request from the link during a timing window (to be defined) before the detection of the subaction gap	Agreed in principle	PHY designers to provide text for rule and proposed timing
7	Cable PHY enhancements - "Caboose" packet	Proposed to be deleted, decision pending on a check that all info now accessible by remote PHY read	Agreed in principle	suspend/resume working group to check
24	Clarifications and corrigenda - Security extensions	In Draft D0.09 - language needs tightening up to be acceptable to legal beagles? Decision to replace “security” by “ rransaction integrity safeguards” 26 Sep 97	Agreed in principle	PJ to modify text. All to solicit further legal review

26	Priority requests for response packet transmission	send response without regard to fairness, if ack_busy received, wait a reset gap, same rules, (i.e. one shot per gap), agreed on 25 sep 97	Agreed in principle	PJ to incorporate into next draft
31	Sleep mode (a.k.a. suspend / resume)	Proposal made by suspend/resume working group agreed in principle 25 Sep 97	Agreed in principle	PJ to integrate proposed text, state machines and C code with existing P1394a draft, but maintain this as a separate document while reviewed by the working group
36	Speed signal sampling requirements	tighter specification required for speed signal in order to ensure interoperability. JS proposal on ftp site as 97-059r0	Agreed in principle	PHY designers to review JS's proposal
51	Token-style Arbitration	Allows optimisation of isochronous transfers in a sub-tree - As described in Bill Duckwall's 1394 optimisations document. NB support for Token Style arbitration should be optional (decided 24 Jun 97)	Agreed in principle	PJ to provide text and state machine modifications
52	Max Bus Hold	Clarify that MAX_BUS_HOLD is guaranteed by the Link, not by the PHY. NB possible confusion with MAX_BUS_OCCUPANCY (no longer defined) and MAX_DATA_TIME	Agreed in principle	PJ to resolve possible confusion and endsure that appropriate text is in the draft
55	Ping timer mechanism	Need an overall description of use of ping timer to set gap counts	Agreed in principle	unassigned to provide text for inclusion in ballot draft or earlier
59	Lreq for multi-speed concat	Links may not be able to transmit Lreq whilst transmitting another packet - propose to allow Iso Lreq up to 10 Sclks after last iso transmit . PHY designers agreed LReq rules - start transmission no later than 1 SClk after IDLE	Agreed in principle	PHY designers to review latest ideas
70	Link to check CYCLE_START	Decided that Link is only required to look at TCode (and checksum) to identify a cycle start packet	Agreed in principle	PJ to prepare wording for review on reflector and include in next draft
74	Electrical specification for S400 serial transmission	EH proposal of 25th September agreed in principle	Agreed in principle	PHY designers to review/ratify proposed specification and accompanying informative text
80	Isochronous bandwidth allocation	lack of clarity	Agreed in principle	PJ to provide clarification text for next draft
81	Maximum isochronous payload	Currently there's a lack of clarity. Agreed that the maximum isochronous packet size will be exactly twice the asynchronous - 26 Sep 97	Agreed in principle	PJ to provide table in next draft
84	Vendor Specific page	Page 7 to be a vendor specific page	Agreed in principle	PJ to update draft
86	Split time out	a minimum should be set (= default), all nodes on a bus share the same split time-out value T label reuse after timeout needs to be specified for the requested and the responder. There should be a guard-band. The bus manager needs to ensure consistent use.	Agreed in principle	PJ to produce a revision 1 of the proposal and put it on the ftp site prior to final approval

87	S100 self-ID	potential race condition, fixed by state machine modification	Agreed in principle	To be confirmed by PHY designers

35	Power distribution, voltages	New clause 6.1 in Draft D0.09 - major revision following recommendations from Power Rangers. 3W allowed “default” power consumption from a cable for a PHY	Agreed	PJ to incorporate into next draft
39	Recommended interval between software-initiated bus reset(s)	Software “should” wait at least 2 seconds	Agreed	PJ to incorporate into next draft
53	PHY behaviour on LPS -> 0	When LPS -> 0 (for longer than 2.75 usec), PHY takes SClk, CTL and DTA to zero.	Agreed	PJ to include trhis explicit statement in next draft

2	PHY/Link interface - PHY register map(s)	In Draft D0.09	Stable	
4	PHY/Link interface - LReq formats	In Draft D0.09	Stable	
5	PHY/Link interface - AC timing	In Draft D0.09 (no objections raised 25 Jun 97)	Stable	
6	PHY/Link interface - PHY-LINK handover	Text in Draft (9X) confirmed 4 Aug - addition of a note on possibly backwards compatibility when using a link which does insert the extra IDLE	Stable	
8	Cable PHY enhancements - Ping packet	In Draft D0.09	Stable	
9	Cable PHY enhancements - ACK-accelerated arbitration	In Draft D0.09, but see 46	Stable	
10	Cable PHY enhancements - Fly-by arbitration	In Draft D0.09, but see 46	Stable	
11	Cable PHY enhancements - Multi-speed packet concatenation	In Draft D0.09, but see 46	Stable	
12	Cable PHY enhancements - Per port disable	Superseded by suspend/resume mechanism	Stable	
13	Isochronous connection management	Clause 9 to be removed- proposed June 24, voted Aug 4th	Stable	
14	Clarifications and corrigenda - Acknowledge codes (ack_tardy)	In Draft D0.09	Stable	

15	Clarifications and corrigenda - Response code usage	In Draft D0.09	Stable	
16	Clarifications and corrigenda - Quadlet vs. block read and write requests	In Draft D0.09	Stable	
17	Clarifications and corrigenda - Command reset effects	In Draft D0.09	Stable	
18	Clarifications and corrigenda - Unit registers (reserved address spaces)	In Draft D0.09	Stable	
19	Clarifications and corrigenda - ROM Bus_Info_Block	In Draft D0.09 Link speed and other items	Stable	
20	Clarifications and corrigenda - Determination of the bus manager	In Draft D0.09	Stable	
21	Clarifications and corrigenda - Automatic activation of the cycle master	In Draft D0.09	Stable	
22	Clarifications and corrigenda - Cycle too long error	In Draft D0.09	Stable	
23	Clarifications and corrigenda - Abdication by the bus manager	In Draft D0.09	Stable	
25	More than 63 nodes	Action on more than 63 nodes. PHY: don’t wrap beyond Node_ID of 63; link treat reception of a Self-ID packet with a Node_ID of 63 as a bus configuration error. Agreed 4 Aug PHY designers revised state machine 25 Aug.	Stable	
27	Bus_Info_Block - bootable device	Bit to indicate "bootable" device. Agreed that this is better solved in the new IEEE 1212 - 4 Aug	Stable	
28	Bus_Info_Block - generation bit	In Draft D0.09 - "Generation" bit - new text in clause 9.7, agreed 25 jun 97	Stable	
29	Bus_Info_Block - max_rec	max_rec to indicate maximum for both read and write. agreed 25 Jun 97	Stable	

30	Length of arbitrated short reset	Length of arbitrated (short) reset signal for long distance PHY and cable issue should be adjusted if necessary. PHY designers agreed that current value is OK for cables up to 50m, so no change.	Stable	
32	PHY/Link reset	Link can reset PHY/Link interface by using LPS low. See also Nos 53, 54 and 57	Stable	See 57
34	Power distribution, agencies	Agency compliance (safety) issues. DWs summary (very brief) is in 97-203r0 on the FTP site. Informative Annex. Text from JB sent to PJ	Stable	
37	How to set the local PHY's gap count	Specified in Draft D0.09	Stable	
38	Formal definition of an ACK packet for arbitration purposes in the PHY	Any 8-bit packet	Stable	
40	Extended speed codes for SPEED_MAP	In Draft D0.09	Stable	
41	"Fairness" optimizations	As per draft D0.9X, with modifications:- Field size is 6 bits (both fields byte aligned); Behaviour is undefined when PRI-REQ is written with a value larger than PRI_PREF.	Stable	
42	Electrical isolation / Annex A	In Draft D0.09 - New Annex A agreed 24 Jun 97. Reconfirmed as normative on 5 Aug 97 (in order to replace the 1394-1995 normative annex)	Stable	
43	Asynchronous streams (tcode 0x0A)	In Draft D0.09 - New Clause 7 agreed 24 jun 97	Stable	
44	PHY/Link interface DC specification	In Draft D0.09 agreed, as no objections raised 25 Jun 97	Stable	
45	Availability of SClk	Defined by LPS rules	Stable	
46	LReq summary table	In Draft D0.09.Issues split out - See 58, 59 60. Speed checking proposal:- Whoever does the concatenation checks the speed. At most one arbitration per LReq. Agreed 4 Aug. Don't include any text which prohibits a PHY from checking a concatenated LReq and performing two arbitrations (thought compliant Links will never generate this)	Stable	
47	PHY/Link interface signals	Draft D0.09. LPS: optional on link, required on PHY LinkOn: optional on link, required on PHY Direct: optional on link, required on PHY - agreed 24 Jun 97	Stable	
48	Ping timer	In the Link - agreed 24 jun 97	Stable	
49	Cable line state	In Draft D0.09 - new RX_TOKEN_GRANT	Stable	

50	Read response for data block	In Draft D0.09 - new text - agreed 24 Jun 97	Stable	
54	Link initialisation of PHY-Link Interface	Possible problem when using an isolation barrier, requiring C/D/LReq to be taken to zero for two cycles when Sclk is seen - agreed that only one cycle is required (PHY meeting 26 Aug)	Stable	see 57
57	LPS specification	LPS means “give me SClk”. LPS AC specification agreed as per presentation by RB/NM on 24 Jun 97. Link can reset PHY-Link interface by taking LPS low (see 32). See 53. See 54. PHY designers agreed spec 26 Aug.	Stable	
58	Isoch LReq	Need tighter defn of “in isoch phase”, as JB presented on 24 Jun 97. PHY designers agreed LReq rules 26 Aug	Stable	
60	Cycle sync after pri req for enhanced arb	Does the link wait for pri req to be serviced or send Cycle sync immediately - agreed the latter, and PHY does not cancel priority request	Stable	
61	Root contention timings	Change ROOT_CONTEND_FAST and ROOT_CONTEND_SLOW times to deal with longer P1394a cables.. Agreed that 1394a will be modified accordingly. PHY designers agreed new numbers 25 Aug	Stable	
62	PHY version registers	As proposed by JF	Stable	
63a	Power-on (hard) reset states for PHY registers	All PHY registers to have defined “power-on/hard reset” states. States agreed by PHY designers 25 Aug	Stable	
64	SPEED_SIGNAL_LENGTH vs SPEED-SIGNAL-TIME	two terms for the same value?	Stable	
65	Lock transactions	Draft 0.9X has new text to deal with issue with future compatibility when performing lock transactions on registers with reserved fields	Stable	
66	BANDWIDTH_AVAIL > S400	If 8.1.2 survives, then calculations in the paragraph on the overhead field need updating (spd and/or xspd)	Stable	
67	Asynch packets at CYCLE_START time	Issue removed by use of new Accelerate/Deaccelerate LReq (see No	Stable	
68	FORCE_ROOT_TIMEOUT	Max value is too large (two long daisychains with either end contending for root). Problem solved by changing other timing constants (PHY designers 25 Aug)	Stable	
69	enab_accel	Revised behaviour - using PHY learning, as per Ganesh Murthy proposal on 24 Jun. Proposal now withdraw, as superseded by new Accelerate/Decelerate mechanism	Stable	
71	Cycle Start starvation	Replace Cycle Sync LReq with two LReqs - Accelerate/Deaccelerate. Default state is Accelerate (but this only applies of enab-accel is also set). Agreed 4 Aug	Stable	

72	gap_count calculation constants when using ping timing	various new constants are required for ping-timer-based gap count calculations - arb_response_delay, link_to_bus_delay, phy_delay (min value), bus_to_link_delay, ping_response_time will be defined as constants, and phy_delay_jitter will be reported. PHY designers agreed definitions and values 25 Aug	Stable	
73	reserved for IEEE purposes	reserved fields should not be considered fair game by other standards or trade association bodies	Stable	
75	SClk specification	Specify as frequency +- 100ppm, plus 40% 60% duty cycle	Stable	
77	PHY legacy register map	Not appropriate to incorporate this into P1394b	Stable	