5. PHY/Link interface specification

5.1 LReq Rules

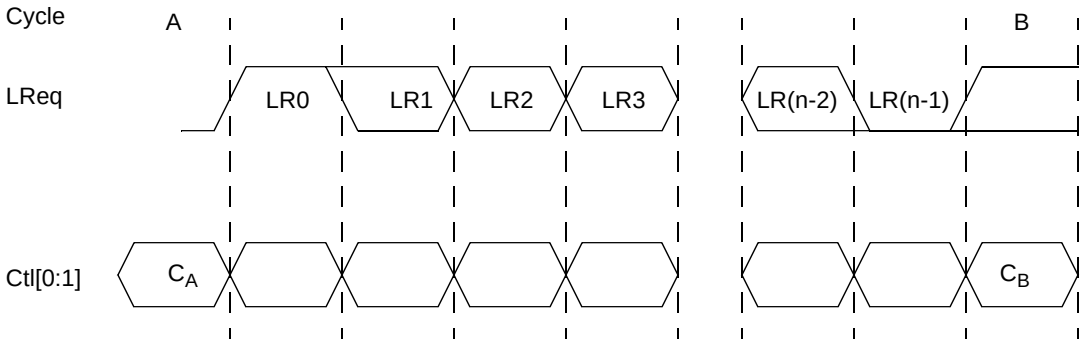

Figure 5-1 — LReq timing

In general, the Link prepares to issue requests asynchronously with respect to activities on the Serial Bus. However, certain requests are allowed only at specific times with respect to bus activity. Even when a request is issued at a valid time,. other activity on the bus may cause the PHY to cancel the request or to pend the request until the other activity has been completed. Rules are necessary (i) to specify when the Link may issue the various requests and (ii) so that the Link may unambiguously determine whether the PHY has cancelled the request or held it pending.

For the purpose of these rules, two specific cycles are defined, denoted as A and B in the above figure. The rules are specified in terms of the values that the PHY is driving on the Ctl[0:1] lines during these two cycles, denoted as C_A and C_B respectively. Cycle A is the cycle immediately before the Link sends the start bit of the LReq. Cycle B is the cycle immediately after the cycle when the Link sends the stop bit of the LReq, and is the cycle in which the PHY commences (and possibly completes) processing the LReq. As the PHY processes the LReq, and/or other events on the bus occur, the PHY will change the status of Ctl[0:1], this will occur some number of cycles after cycle B.For some values of C_B, the link therefore continues to monitor Ctl[0:1] until the PHY changes the value to one which determines the dispotision of the LReq.

Some LReqs are permitted to be issued when the Link has control of the bus, during which time C_A and possibly C_B are not relevant.

The rules for issuing the various LReqs are given in the following table:-

Table 5-1 — Valid times for issuing an LReq

Link Request	Permitted when PHY has control of the bus and the value of C_A is	Permitted when Link has control of the bus?	Comment
Fair	IDLE, Status	No	
Priority	IDLE, Status	No	

Table 5-1 — Valid times for issuing an LReq

Link Request	Permitted when PHY has control of the bus and the value of C_A is	Permitted when Link has control of the bus?	Comment
Immediate	Receive, IDLE or Status (see comment)	No	The start bit of an immediate request may be transmitted up to 2 SClk cycles after Ctl[0:1] goes IDLE following packet reception, by which time a status transfer may also have started Sent after destination_ID decode during packet reception to prepare for ACK transmission
Isochronous	Receive IDLE or Status (see comment)	Yes	The start bit of an isochronous request may be transmittted up to 2 SClk cycles after CTL[0:1] goes IDLE following the reception or transmission of a previous isochronous packet or cycle start packet. Note that a status transfer in response to a read register request may also have started by this time. Sent during an isochronous period when the link is ready to transmit an isochronous packet
Register read	Receive, IDLE or Status	Yes	May not be issued when there are pending register read requests
Register write	Receive, IDLE or Status	Yes	
Cycle sync	Receive, IDLE or Status	Yes	Cycle sync may only be issued by cycle slaves, and is issued once every isochronous period, as soon as possible after the local clock indicates the start of a new isochronous period.

In general, the PHY behaviour will vary depending on whether another transaction on the bus is detected before it has succesfully completed processing the LReq.

The Link may determine the PHY treatment of the LReq by monitoring the value of Ctl[0:1] during cycle B and during subsequent cycles, as shown in the following table:-

Table 5-2 — PHY disposition of LReq

Link Request	Ctl[0:1] at B or later	PHY status/Link action
Fair, Priority	Receive	If arbitration acceleration is enabled, and the incoming packet is an ACK, then request retained, otherwise request discarded as soon as the PHY determines that the incoming packet is an ACK (EDITORIAL NOTE: C code needs correcting to reflect this behaviour) Request always discarded if arbitration acceleration is not enabled
	Transmit	Arbtration won, link may start to transmit a packet
	IDLE or Status	Request retained unless status reports a reset, continue to monitor Ctl[0:1]
Immediate	Transmit	Link may start to transmit the ACK packet
	Receive	(Error condition, cannot occur)
	IDLE or Status	Request retained unless status reports a reset, continue to monitor Ctl[0:1]
Isochronous	(Link has control)	wait until Link releases the interface, and monitor for the next change on Ctl[0:1]
	Transmit	Arbitration won, Link may start to transmit the packet
	Receive	Arbitration lost, request retained by PHY and will be retried at the next available opportunity, wait for the next change on Ctl[0:1]
	Status	Request discarded if Status indicates subaction gap (this is an error condition and should not occur), otherwise request retained unless status reports a reset, wait for next change on Ctl[0:1]
	IDLE	Wait for the next change on Ctl[0:1]

Table 5-2 — PHY disposition of LReq

Link Request	Ctl[0:1] at B or later	PHY status/Link action
Register read	(Link has control)	Wait until Link releases the interface, and monitor for the next change on Ctl[0:1]
	Transmit	Request retained. Bus request LReq was previously issued, and now takes priority.
	Receive	Request retained.
	Status at B	A status transfer is already in progress in response to an asynchronous event on the bus, which will be terminated by IDLE, or interrupted by receive. The request is retained unless status reports a reset.
	Status	PHY response to the request. Note that the request is “retained” until it has been completely sent to the Link. Note also that status is normally terminated by IDLE, but may also be terminated by Receive. Note that an interrupted status from a previous asynchronous bus event will be combined into the status provided in response to the register read
	IDLE	Wait for the next change on Ctl[0:1]
Register write	Any	Request completed
Cycle sync	Any	Request completed. Note that the PHY will NOT cancel a retained priority request (but will it cancel any other sort of bus request??)

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