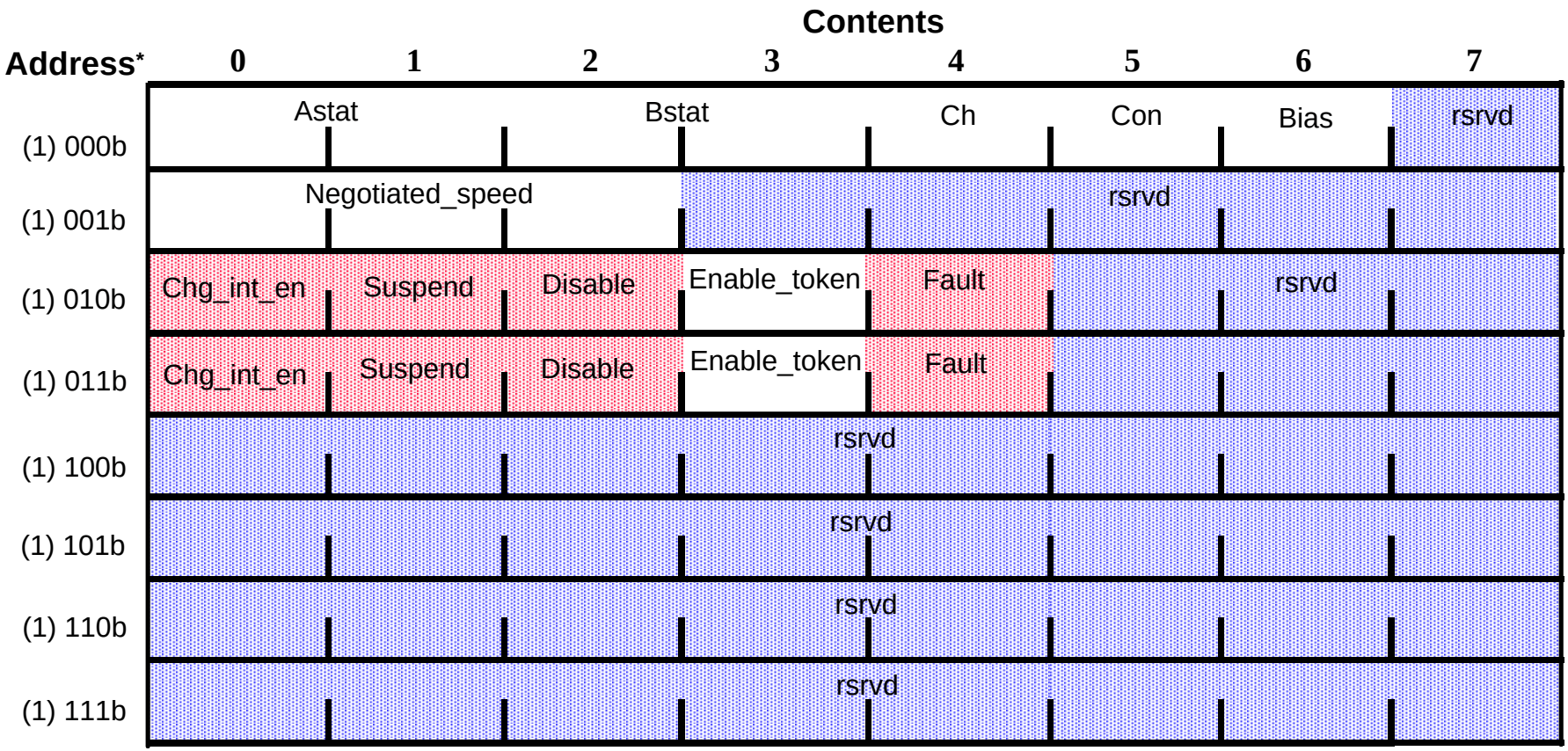
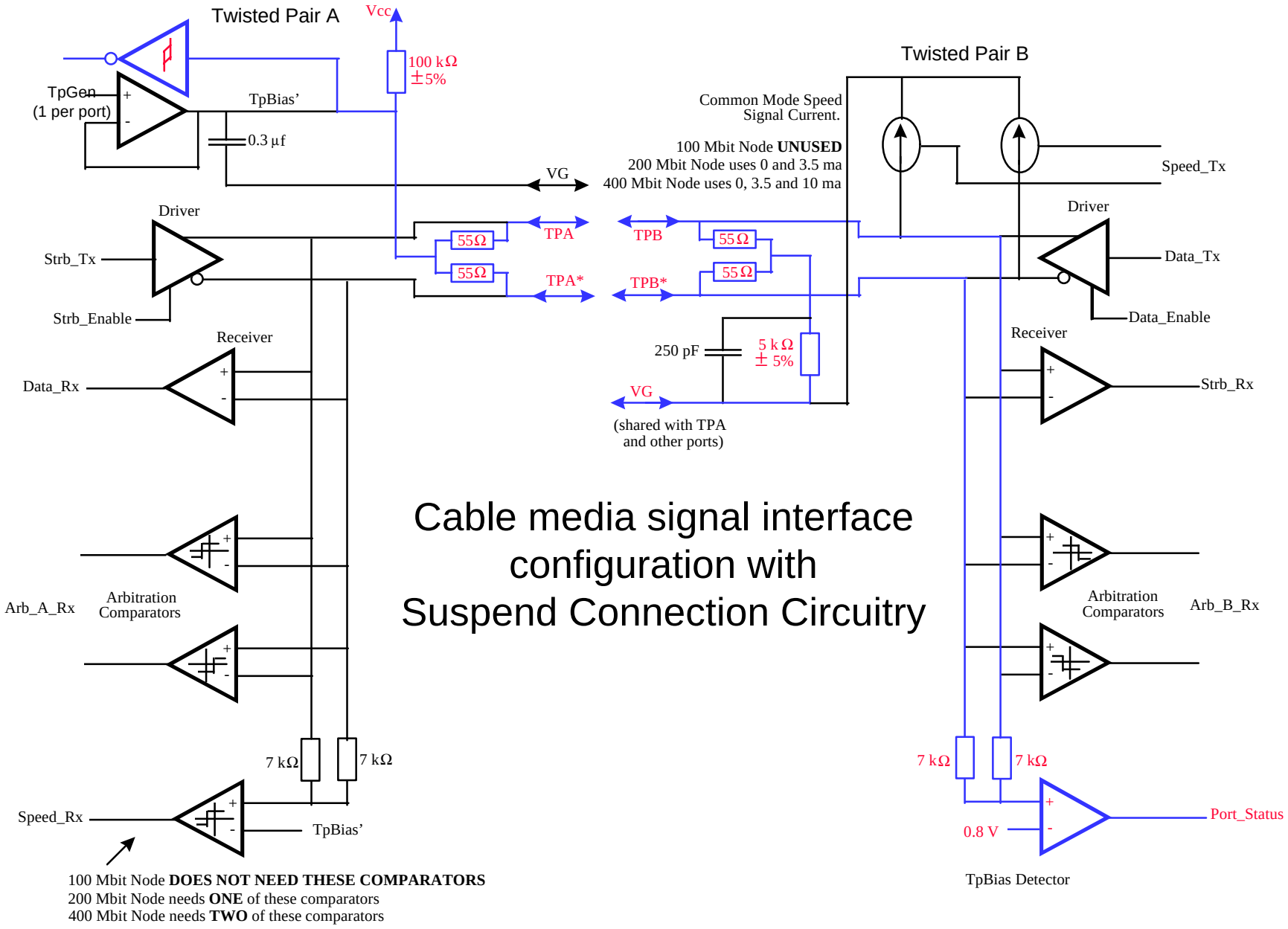
PHY Port Register Map



*The most significant bit of the address is used only by the link during a PHY register write (Lreq). The most significant bit is **not** used when addressing a port via an extended PHY packet.

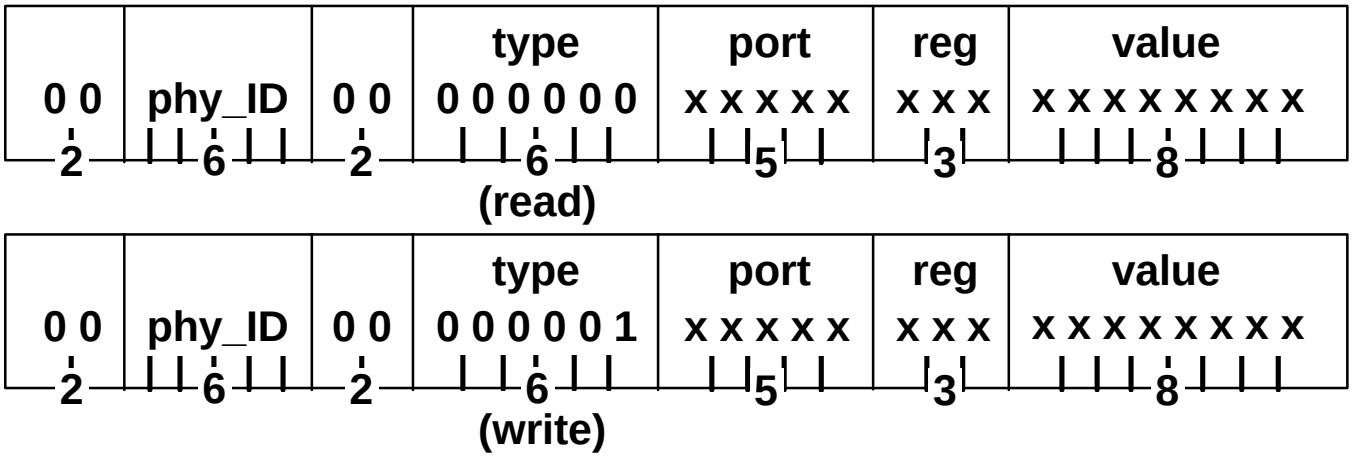
Register: (1) 010b and (1) 011b - ***Control Set*** and ***Control Clear*** (respectively)

FIELD	SIZE	TYPE	DESCRIPTION
Chg_int_en			***ch****ang****e*** ***int****errupt* ***en****able* - if set, the PHY will interrupt the link with a Status Packet when one or more of the following bits change state: ***Con***, ***Bias***, ***Suspend***, ***Fault***, or ***Disable***; this bit is clear subsequent to a power reset;
Suspend			When writing this bit at register ***Control Set***, the bit does **not** set, however, the write operation will select the poer as a suspend initiator; writing this bit a register ***Control Clear*** will **not** clear this bit, however the write operation will select the port as a resume initiator; this bit is set subsequent to a power reset.
Disable			When set, a port is disabled (placing th port in a low power state similar to suspend); a disabled port will not respond to or generate bus resets, suspend notification, or resume events; this bit is clear subsequent to a power reset.
Enab_token			Enable token-style arbitration. When set, the enhancements specified in clause 6.5 of the IEEE 1394-1995.A draft specification shall be enabled for this port.
Fault			set when a port is not able to successfully interact with its connected port during either a suspend or resume process; this bit is clear subsequent to a power reset.
Rsrvd			reserved - must not be used or interpreted as having a meaningful value.



Cable media signal interface configuration with Suspend Connection Circuitry

PHY Register Addressing
extended PHY Packets



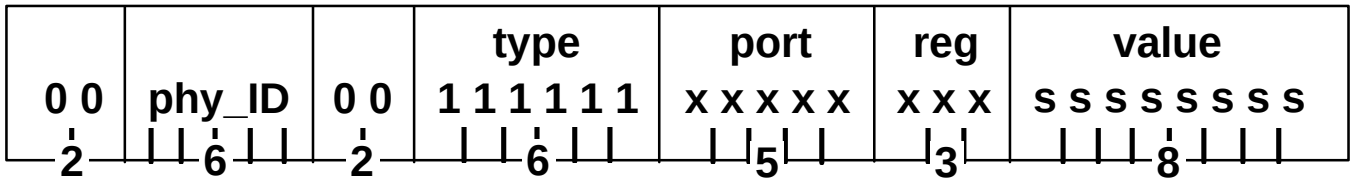
phy_ID: 6-bit node address of the ports PHY

port: 5-bit port select value. Values 0-26_{10} inclusive select select a speciic port in a node; values 27_{10} though 30_{10} are reserved; value 31_{10} selects the 8 node registers;

reg: 3-bit register select field used to address a particular port or node register;

value: 8-bit field which either returns contents of the selected register during read or contains a pattern of bit(s) to be set or cleared during register write

PHY Response Packet



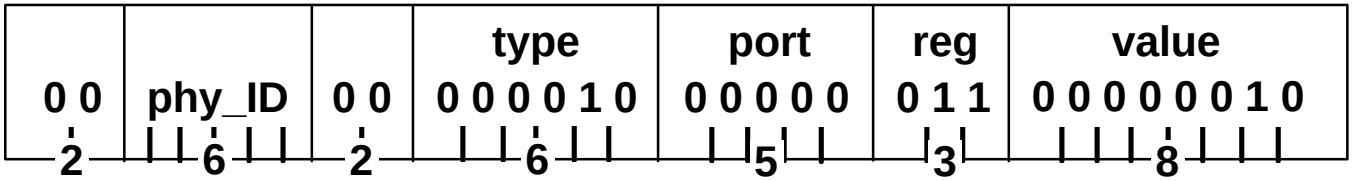
phy_ID: 6-bit node ID of node generating the response packet

port: 5-bit port register value (same as the port register value provided in the extended PHY packet for which the response is being generated);

reg: 3-bit register value (same as the register value provided in the extended PHY packet for which the response is being generated);

value: 8-bit status currently contained in the addressed by the port and reg fields. If an invalid (e.g. reserved) register is addressed, the value will be zero for all bits.

Extended PHY Packet
Type “RESUME”



phy_ID:	6-bit node ID of node generating the packet
type:	000010b (**RESUME)**
port:	5-bit port register value = 00000b;
reg:	3-bit register value = ***Control Clear*** (011b);
value:	00000010b (***Suspend*** bit set).

1394 Bus Topology Example
Revision 0.03 July 14, 1997