CONGRUENT SOFTWARE, INC.
3998 Whittle Avenue
Oakland, CA 94602
(510) 531-5472
(510) 531-2942 FAX

FROM: Peter Johansson

TO: IEEE P1394a Working Group

DATE: September 27, 1997

RE: Minimum SPLIT_TIMEOUT values

Disk vendors have raised concerns in the T10 SBP-2 working group that they may not be able to support split time-out values below some minimum value.

Independently, I believe that all nodes on a bus need to share the same split time-out value and that the responder's behavior after expiration of the time-out needs to be specified.

I propose the following for section 9 of P1394a.

9.x SPLIT_TIMEOUT register

The SPLIT_TIMEOUT registers set the default timeout value for detecting split-transaction errors. The value of SPLIT_TIMEOUT sets the maximum time for the receipt of a response subaction after the transmission of a request subaction. After this time, a responder shall not transmit a response for the request subaction and a requester shall~~should~~ terminate the transaction with a ~~response_timeout~~request status of TIMEOUT. For a requester the time-out period commences when an *ack_pending* is received in response to a request subaction. A responder starts the time-out period when an *ack_pending* is transmitted. Figure9-x illustrates the portions of the SPLIT_TIMEOUT register implemented on Serial Bus.

NOTE— A requester should not reuse the transaction label from an expired request subaction in a subsequent request subaction to the same node unless at least twice the split time-out period has elapsed since the initiation of the expired subaction.

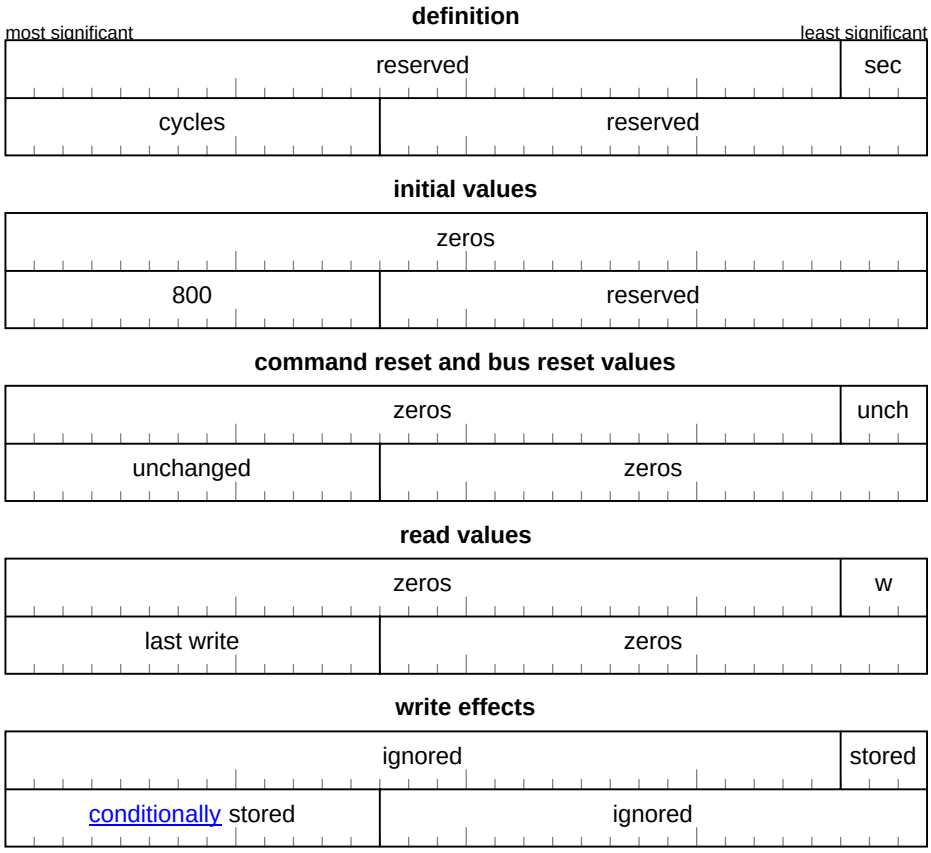

Figure 9-x – SPLIT_TIMEOUT format

The *sec* field, in units of seconds, and the *cycles* field, in units of 125 µs, together specify the time-out value. The value of *cycles* shall be less than 8000. The bus manager, if present, shall insure that all nodes on the bus have identical values in their SPLIT_TIMEOUT registers.

The minimum timeout value is 0.1 second. If a value smaller than this is written to the SPLIT_TIMEOUT register it may be ignored or rounded up to 0.1 second.

~~Since the Serial Bus SPLIT_TIMEOUT_HI register implements only the three least-significant bits, the timeout can be no longer than 8 s.~~

~~The Serial Bus SPLIT_TIMEOUT_LO register implements only the 13 most-significant bits. These bits specify a fractional value of a second in units of 1/8000 s, rather than 1/8192 s as specified by the CSR Architecture. The timeout resolution is nominally 125 ms.~~

NOTE— The Serial Bus definition of the SPLIT_TIMEOUT register is different from that defined within the CSR Architecture. Serial Bus interprets the most significant 13 bits of the SPLIT_TIMEOUT_LO register as units of 1/8000 s, rather than a true binary fraction of a second with units of 1/8192 s. Since precise timeouts are not necessary, applications may ignore this difference when calculating values for use within the SPLIT_TIMEOUT_LO register.