Proposal for IEEE 1934a Supplement

#### Problem Statement

- Some older S100 PHY designs based on Apple licensed core logic cannot reliably receive packets with minimum data-prefix of 140ns
- Receiver logic enabled too late causes first 2 to 4 bits to be missed

#### Problem Statement (cont.)

- These PHYs are in existing consumer products
- These PHYs require at least 180 ns of data-prefix preceding clocked data in order to receive packets reliably (including self-ID packets)

#### Proposal Statement

New timing constant added to Table 7-7:

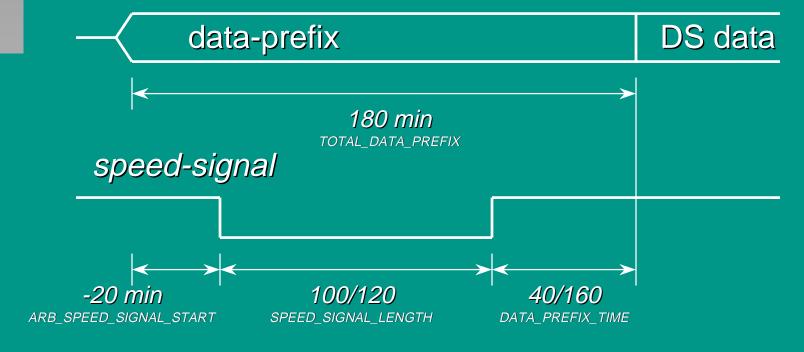
Min Max Comment

TOTAL\_DATA\_PREFIX 180ns

Total data-prefix arbitration signal preceding clocked data (including during speed-signal time)

#### Packet Data-Prefix Timing

serial-bus arb/data



#### *Implementation*

- Increase data-prefix time before speedsignal, or
- Increase data-prefix time after speedsignal and before clocked data, or
- Both of above

#### *Impact*

- Max throughput reduced slightly for a 64 bit S400 packet, min possible transmission time increased from 560 ns to 600 ns
- All currently available and planned TI PHYs generate at least 180 ns of dataprefix preceding clock data