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TO: IEEE P1394a Working Group

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RE: Mandatory *vs.* optional, PHY *vs.* link *etc.*

This memorandum is an initial analysis of Draft 1.1 of P1394a to separate *hardware* implementation requirements according to their domain and whether they are mandatory or optional. Software requirements, such as constraints on the bus manager or the behavior of the transaction or application layers are not summarized in the tables below.

Table 1 – Mandatory P1394a features

Domain	Feature
All PHYs	PHY/link interface
Backplane PHY	PHY register map
Cable PHY	ACK-accelerated and fly-by arbitration
	PHY register map Core registers, bits and fields (figure 6-1 and table 6-1) Port Status page(s) for each port implemented Vendor Identification page
	Self-ID packet(s) in response to the "ping" packet
	Timing constants
Link	Automatic cycle master activation
	Cycle start format and recognition
	Isochronous period too long
	Transaction integrity safeguards
Node	Power distribution and consumption

Table 2 – Optional P1394a features

Environment	Feature
Cable PHY	Self-ID packet 8 ("caboose"); mandatory if nonzero information present
	Some parts of the PHY register map Enab_token in the Port Status page Vendor-dependent page
	Suspend / resume (details to be determined)
	Token style arbitration
Link	Asynchronous streams
	FAIRNESS_BUDGET (priority arbitration for requests)
	Priority arbitration for responses
Packaging	Alternative media attachment (4-pin cable and connector variants)

When we reach consensus on the tables above I suggest we examine how P1394a links and PHYs report their compliance.