# LinkOn Behavior (rev 0.1)

## *Goal of LinkOn*

The goal of the LinkOn pin from the PHY to the Link is for the PHY to provide the Link or other power management controller with a message which indicates that the 1394 link and transaction layers should resume from a low power state to begin processing packets. The PHY indicates a LinkOn in response to specific conditions on the 1394 bus. For information on the 1394 bus specific condition, refer to section XXX (Suspend/Resume section).

A LinkOn message received from a PHY will generally cause a power management event inside of the attached system. This event is an interrupt to the system, and will cause a resume event.

## *Missing Items from Current Description*

The current draft of this description is very brief. Items that need to be addressed:

- All AC Timings
- Isolation toggling period for LinkOn
- Min/Max Timing of resume event on the port to LinkOn assertion

## *LinkOn Event*

In order for the Link or other power management controller to correctly interpret a LinkOn event, LinkOn needs to have simple rules. This is necessary as much of the system will be powered off at this point, and will either have no clock or a very slow clock, such as the 32 kHz clock used for clocking the RTC (real time clock) circuitry of a PC.

As such, the LinkOn pin on a PHY should behave similar to an interrupt. When no LinkOn message is to be sent, the LinkOn signal should be in a stable, known state, preferably at 0V for lowest possible power consumption. When the link is to be resumed, the LinkOn pin should be in the opposite state. To support LinkOn through an isolation barrier, this opposite state should toggle similar to LPS described in XXXX. (wave form for LPS rule).

Since it is essentially an interrupt, the LinkOn pin should not be multiplexed with other logic in functional mode. It should be a dedicated output from the PHY. This allows for the most straightforward processing. During power on reset, this pin may be multiplexed with other logic, as the link should not be looking at LinkOn events at this time.

## *LinkOn Waveform*

The waveform for LinkOn is shown below.

**Figure 1: LinkOn Waveform**

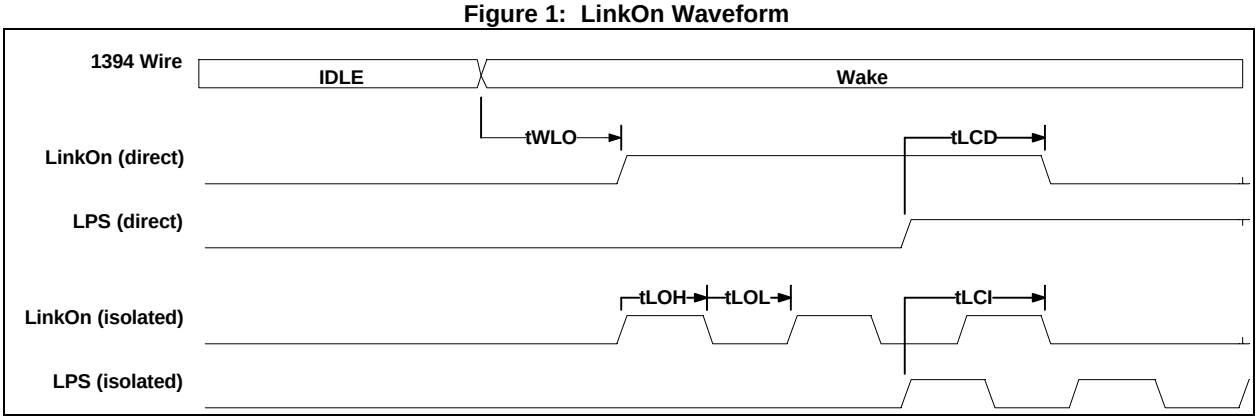

**Table 1: LinkOn Timing Parameters**

| Parameter | Description | Min | Max |
|---|---|---|---|
| tWLO | Time from wake event detected on 1394 wire to LinkOn signaled. | ? | ? |
| tLCD | Time from LPS asserted to LinkOn cleared (direct interface) | ? | ? |
| tLCI | Time from LPS asserted to LinkOn cleared (isolated interface) | ? | ? |
| tLOH | LinkOn High Time (isolated interface) | ? | ? |
| tLOL | LinkOn Low Time (isolated interface) | ? | ? |

## *Other LinkOn Rules*

LinkOn is only signaled by the PHY when LPS is low.. When a LinkOn condition is seen, the LinkOn pin will be set to an active high level (direct) or toggling (isolated). It is up to higher level software to enable the link (or other receiving device of LinkOn) to generate a wake up event to the rest of the system.

When LPS is sent active by the Link, this is an indicator to the PHY that the message has been received and the Link circuitry is active. At this point, the LinkOn message can be cleared.