Per Port Speed Mapping

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Configuration Management

- Imagine a 6-port PHY with internal routing to the front, back and internals of a box
  - the applications and performance expectations of the “walkup” connections on the front of the box require S100 or S200
  - the internal interconnect requires S400 or above
  - the rear connections might require S400 or above

Configuration Management

- Cost effective routing of 1394 interconnections is critical
  - the “walkup” connection might have to be limited to S100 due to routing losses
  - the PHY location can only be sub-optimal
  - the PHY to Link interface offers limited flexibility and routability

Configuration Management

- Imagine a portable device that MUST run at the same 1394 speed when operating from the battery or the wall plug
  - an unnecessary restriction with serious performance limitations
    - many applications will utilize asynchronous data
- Battery duration may be compromised to support docking performance

Goal and Objective

- P1394a should provide a mechanism that supports multiple programmable speed maps through a multiported PHY
- Bring this into the scope of P1394a
- Enlist the support in interested parties to create a task group and draft the required changes

Today's Situation

- A PHY can only have one speed map
  - that speed is usually set at the maximum supported by the PHY
- The current definition lacks necessary flexibility
- Systems will have to be compromised or increased in costs to satisfy potential applications

How Did We Get Here?

- We started with a simple view of the network topology and behaviors
- These assumptions that are no longer valid
- Flexible configurations and portable applications require more flexibility

Available Options

- Leave the specification as it is and drive up the cost of complex nodes
  - adds $’s to the cost of multiport solutions
- Limit the options for battery powered management
  - a notebook can only run at one speed when docked or portable

Recommendation

- Bring multispeed into P1394a
- Programmable devices will present their slowest speed mapping to the 1394-1995 speed map mechanism
- Bring a standardized method into P1394a to manage the maximum speed of each port in a multiported configuration
- Redefine the speed mapping function to support multiple speeds through a node