From: Steve Finch, steve_finch@tus.ssi1.com
To: P1394a Working Group
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Subject: Misleading information in clause 5 about S25 and S50

Clause 5 describes the Phy/Link interface and does a very good job of covering this interface for S100, S200 and S400. Unfortunately, this can not be said for its treatment of S25 and S50 speeds associated with backplane operation. In fact, the only references I could find for S25 and S50 were the following:

1. In Clause 5, the paragraph under figure 5-3 reads:

   "The interface described in this section supports data rates of S100, S200 and S400 in the cable environment and S25 and S50 in the backplane environment. In the timing diagrams in this section, each bit cell represents one clock sample time. The specific clock-to-data timing relationships are described in clauses 5.6.2 and 5.6.3."

2. In Table 8-1—Maximum data block payload for asynchronous primary packets

3. In Table 9-1—Maximum payload for isochronous stream packets

In fact, Clause 5 has statements that are inconsistant with at least S25 mode of operation. For example, the second paragraph of Clause 5 reads:

> "The interface specified in this section is a scalable method to connect one Serial Bus link chip to one Serial Bus PHY chip. The width of the data bus scales with the highest speed both chips can support, using two signals per 100 Mbps. The clock rate of the signals at this interface remains constant, independent of speed, and supports isolation for implementations where it is desirable."

We can either fix Clause 5 to allow/describe the Phy/Link interface for S25 and S50 modes or (and this is my preference) we can eliminate the reference in the paragraph quoted in (1) above. If we do this, I would suggest adding the following somewhere:

"This clause applies to devices which support speeds of S100, S200 and S400 only. IEEE 1394-1995 also defines speeds of S25 and S50 for backplane implementations, refer to that specification for relavent information."