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To: P1394a Working Group
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Subject: Discrete Link Interface Requirements

Clause 5 of P1394A Rev. 1.1 contains the following paragraph:

"With the exception of D[0:7], discrete PHY implementations shall support all of the PHY signals shown in figure 5-1. The number of data bits implemented depends upon the maximum speed supported by the PHY. Discrete link implementations shall implement D[0:7], Ctl[0:1], LReq and SClk. Link support for the other signals is optional. These signals are described by table 5-1."

This states that PHY devices can limit their pin count based upon their maximum speed capability. I think we need to allow link devices to exist which also only support limited speed capabilities. The above paragraph forces link devices to implement all eight bits of the data bus (D[0:7). I would like to see the above paragraph replaced with:

"With the exception of D[0:7], discrete PHY implementations shall support all of the PHY signals shown in figure 5-1. The number of data bits implemented depends upon the maximum speed supported by the PHY.

Discrete link implementations shall implement Ctl[0:1], LReq, SClk and, at a minimum, D[0:1]. The number of data bits implemented depends upon the maximum speed supported by the link. Link support for the other signals is optional. These signals are described by table 5-1."