# 500 Volt Capacitive Isolation Barriers

## -December '97 P1394a/b meetings-

# LAN versus SCSI?

- **SCSI/Parallel/Serial Port**
  - Short cable runs, local peripherals only
  - Copper shields tie directly to the PC bulkhead
  - Same Green Wire ground assumption
  - Ground loops, galvanic isolation are ignored
- **LAN's**
  - Long cable runs, daisy chains of boxes, distant peripherals
  - Green Wire grounds are uncontrolled
  - Full galvanic isolation for fire and shock hazard elimination
    - » 500 Volts isolation barrier required
    - » Double fault protection, i.e., no single component failure hazards the box
- **1394a/b**
  - LAN or SCSI?
  - This is a "religious" issue

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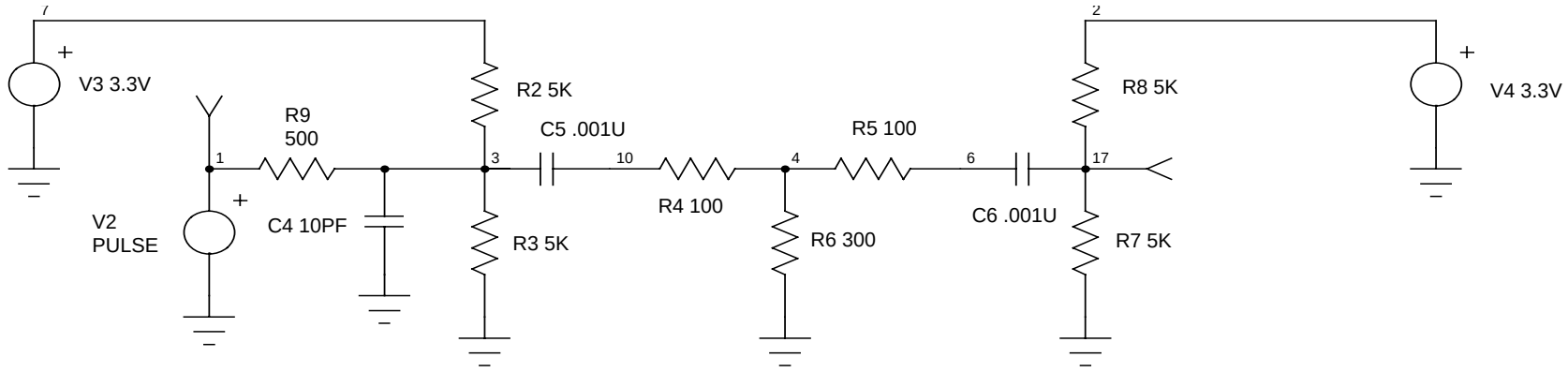
*500 Volt Capacitive Isolation*

# IEEE 1394-1995 Example Barrier

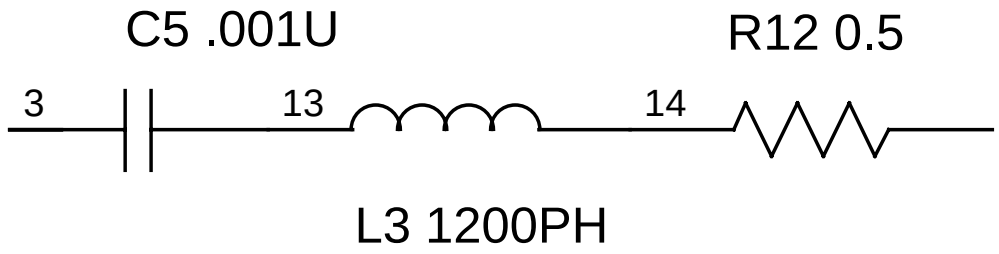



**Simplified Stimulus Circuit** **Capacitive Barrier** **Receiver Circuit**



Eric Hannah/Intel

# Capacitor Modeling




Inductance – Inductance is simply a function of path length and aspect ratio. A 1206 package measures around 1200pH regardless of capacitance, voltage rating and dielectric.

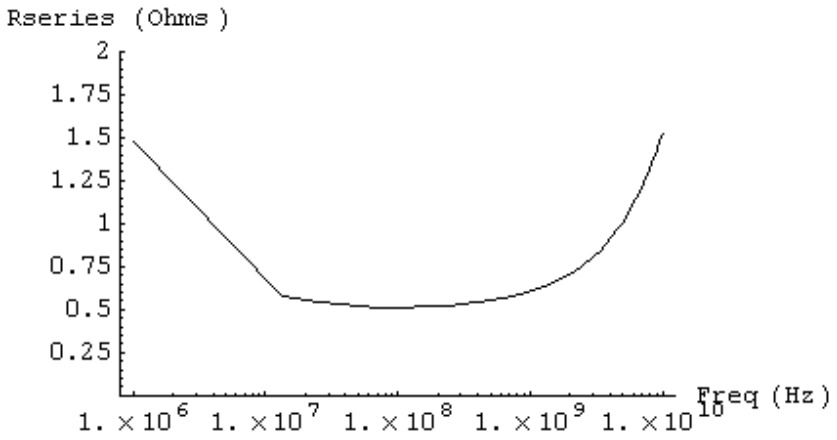
$$R_{Series} = R_{ESR-resonance}\left(1+10^{\left(\left|\log(f / f_{res})\right|-x\right)}\right)$$

$$x \sim 1.6 \; to \; 1.8$$

| Equivalent Series Resistance | Capacitance | Max. Volt | Resonant Freq. | Inductance |
|---|---|---|---|---|
| 500 mOhms | 1000 pf | 500 Volts | 145 MHz | 1200 pH |
| 300 | 2200 | 500 | 98 | 1200 |
| 850 | 2200 | 50 | 98 | 1200 |

(Data for capacitor part: 12067C102MAT2A)

# Equivalent Series Resistance

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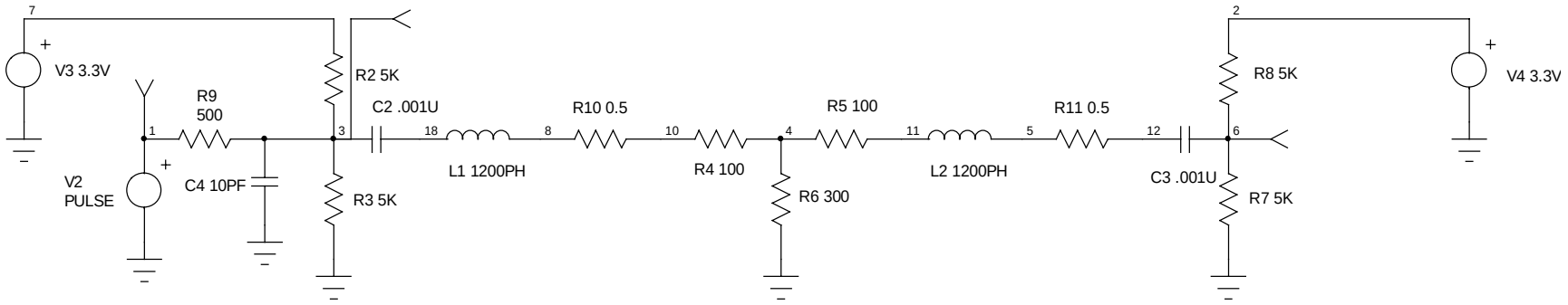
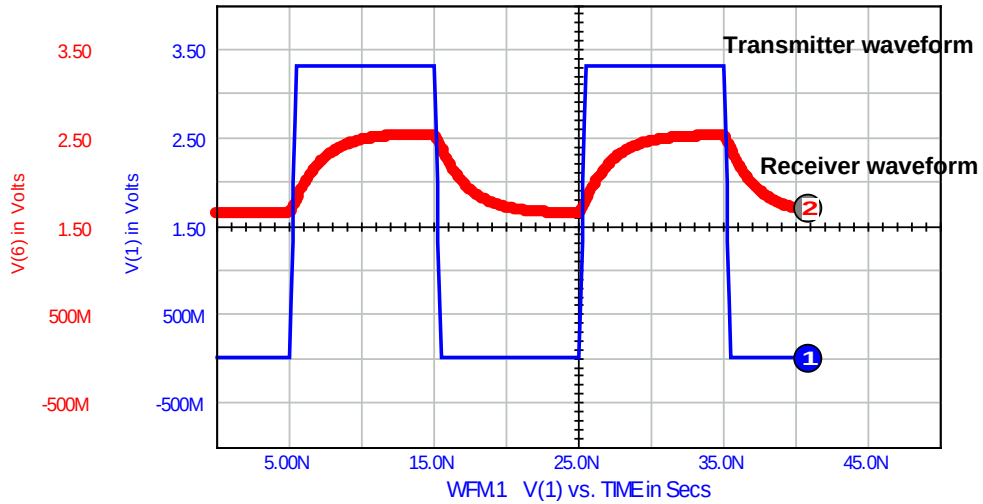
# Realistic Capacitive Barrier




**Spice Simulation**



Eric Hannah/Intel

# Capacitive Barrier Comments

- **We see the ~2 ns delay time in propagating signals across the isolation barrier.**
  - **The source of this delay time is not, however, the isolation barrier. To create a finite delay time it was necessary to "soften" the signal source's waveform with an RC circuit. 500 Ohms and 10 pF were chosen to reproduce TI's data sheet pin specifications for test loads and maximum output current.**
  - **An ideal waveform would cross the isolation barrier with no delay time. Perhaps the mere physical presence of the circuit elements, e.g., the capacitors and resistance networks, add enough capacitance to ground to account for this observation in real systems.**

- **The isolation barrier's internal time constants are irrelevant for delay times.**
  - **RC ~ 100 ns and L/R ~ 10 ps.**
  - **Since the capacitor's self-resonance frequency is around 100 MHz and our logic signals change on a 20 ns time scale we see that actual capacitors in the barrier circuit act as inductors for the high frequency components of the logic signals.**

- **In any case it is clear that using high voltage capacitors (and even doubling them up in series for double fault protection) will have no tangible effect on PHY to LINK signaling.**