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FROM: Peter Johansson

TO: IEEE P1394a Working Group

DATE: November 21, 1997

RE: PHY/Link interface reset and LinkOn behaviors

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This document is a joint contribution from Richard Baker, Jerry Hauck, Prashant Kanhere, Jim Skidmore, Colin Whitby-Strevens and myself. We met, some in person, some by telephone, on November 13 and developed these proposals.

The recommendations were subsequently reviewed by an informal group of link and PHY silicon designers (*aka* the “PHY dogs”) and are presented to the full working group without warranty but with some diligence. Technical issues have been raised that are not yet resolved in this document.

The proposal takes the form of changes to the first part of section 5 in IEEE P1394a Draft 1.2 followed by two new clauses, “Initialization and reset” and “Link-on indication”. There is also a suggestion to modify the description of the Link_active bit in the PHY registers to permit a hardware strapping option for its power reset value.

Of particular interest is the proposal to signal the completion of the PHY/link interface reset. The PHY asserts *Receive* on Ctl[0:1] and data prefix on D[0:*n*] for at least one cycle. The link shall not use the resumed interface (*i.e.*, issue any new requests *via* LReq) until this handshake completes.

In addition, if this proposal is adopted I would make editorial changes throughout section 5 to refer to the Direct pin instead of references to an optional isolation barrier. These changes are recommended because the state of Direct does not unambiguously indicate the presence or absence of an isolation barrier.

# 5. PHY/Link interface

This section standardizes the PHY/link interface previously described in an informative annex of IEEE Std 1394-1995. It specifies the protocol and signal timing. It does not describe specific operation of the PHY except for behavior with respect to this interface.

The interface specified in this section is a scalable method to connect one Serial Bus link chip to one Serial Bus PHY chip. It supports data rates of S25 and S50 in the backplane environment and S100, S200 and S400 in the cable environment. The width of the data bus scales with Serial Bus speed: two signals support speeds up to 100 Mbps while at faster speeds a total of two signals per 100 Mbps are necessary. The clock rate of the signals at this interface remains constant, independent of Serial Bus speed. The interface permits isolation for implementations where it is desirable.

The interface may be used by the link to transmit data, receive data or status, or issue requests. The link makes requests of the PHY *via* the dedicated LReq signal. In response, the PHY may transfer control of the bidirectional signals to the link. At all other times the PHY controls the bidirectional signals.

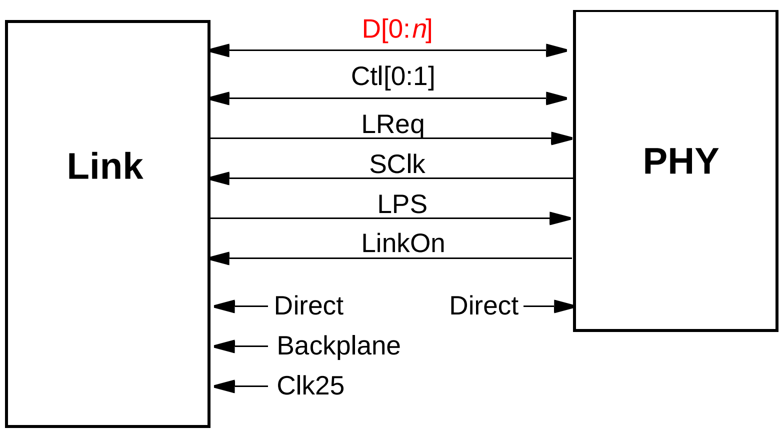


**Figure 5-1 — Discrete PHY/link interface**

~~With the exception of D[0:7],~~ Discrete PHY implementations shall support all of the PHY signals shown in figure 5-1. ~~The number of data bits implemented depends upon the maximum speed supported by the PHY.~~ Discrete link implementations shall support D[0:*n*], Ctl[0:1], LReq and SClk; link support for the other signals is optional. For both PHY and link, the number of data bits implemented, *n*, depends upon the maximum speed supported by the device. The PHY/link interface signals are described in table 5-1.

**Table 5-1 — PHY/link signal description**

| Name | Driven by | Description |
|---|---|---|
| D[0:*n*] | Link or PHY | Data |
| Ctl[0:1] | Link or PHY | Control |
| LReq | Link | Link request ~~port~~ |
| SClk | PHY | 12.288, 24.576 or 49.152 MHz clock (synchronized to the PHY transmit clock) |
| LPS | Link | Link power status. Indicates that the link is powered and functional |
| LinkOn | PHY | Occurrence of a link-on event. ~~Once asserted it shall remain asserted until LPS is asserted and Link_active is TRUE.~~ |

**Table 5-1 — PHY/link signal description (Continued)**

| Name | Driven by | Description |
|---|---|---|
| Direct | Neither | Set high to disable differentiator outputs for the Ctl[0:1], D[0:*n*] and LReq signals.<br>~~Set high to indicate a direct connection or low to indicate an isolation barrier between the link and PHY.~~ |
| Backplane | Neither | Set high if backplane PHY |
| Clk25 | Neither | Meaningful only if Backplane is high. Set high to indicate a 24.576 MHz SClk; otherwise 12.288 MHz.<br>~~Set high to notify the link that SClk is 24.576 MHz~~ |

Data is transferred between the PHY and link on D[0:*n*]. The implemented width of D[0:*n*] depends on the maximum speed of the ~~connected PHY~~ device: 2 bits for S100 or slower, 4 bits for S200 and 8 bits for S400. At S100 or slower, packet data is transferred on D[0:1], at S200 on D[0:3] and at S400 on D[0:7]. Implemented but unused D[0:*n*] signals shall be driven low by the device that has control of the interface.

EDITOR—Is any part of the first deleted paragraph below necessary elsewhere in section 5?

~~In the timing diagrams in this section, each bit cell represents one clock sample time. The specific clock-to-data timing relationships are described in clauses 5.6.2 and 5.6.3.~~

~~The Ctl bus signals control information and is two bits wide.~~

The LReq signal is used by the link to request access to Serial Bus for packet transmission, to read or write PHY registers or to control arbitration acceleration.

The presence of a stable SClk signal generated by the PHY is necessary for the PHY/link interface to be operational. The LPS signal may be used by the link to disable SClk or reset the interface, as specified in clause 5.1.

The LinkOn signal permits the PHY to indicate an interrupt to the link when the link is not active. The details are specified in clause 5.2.

The Direct input controls differentiators on the D[0:*n*], Ctl[0:1]~~, SClk, LPS, LinkOn~~ and LReq signals. When set high it shall disable differentiator outputs on these signals.

NOTE—Differentiators may be required when the PHY and link are connected through an optional isolation barrier.

When a backplane PHY is connected to a link the Backplane input shall be strapped high. The Clk25 input is meaningful only to indicate the SClk frequency generated by a backplane PHY. In the backplane environment, data transfers use D[0:1]. SClk is used to clock the transfers at either 12.288 MHz (for TTL applications) or 24.576 MHz (for BTL and ECL applications). This yields PHY data rates at the backplane of S25 and S50, respectively.

EDITOR—It's been suggested that the following paragraph be relocated between the first and second paragraphs of current clause 5.4, "Transmit", in P1394a Draft 1.2 and that the second note in that clause be deleted.

Whenever control of the bidirectional signals is transferred between the PHY and link, the device relinquishing control shall drive Ctl[0:1] and D[0:*n*] to logic zero levels for one clock before releasing the interface; this is so an optional differentiator circuit can operate properly. This also permits both devices to act upon registered versions of the interface signals while allowing the new owner a clock cycle in which to sample and respond. Note that when the link transfers control to the PHY without a *Hold* request, an additional clock with logic zero on the control and data signals is necessary so as not to place the signal lines in a high impedance state before the PHY takes control. This precaution is important in the absence of an optional isolation barrier between the PHY and link.

## 5.1 Initialization and reset

The optional LPS signal requests the PHY to disable or enable the PHY/link interface. The output characteristics of LPS, if provided by the link, depend upon the state of the Direct input. When Direct is low, LPS is a nominal 300 KHz pulsed output while logically active. The characteristics of LPS are specified by figure 5-2 and table 5-2.

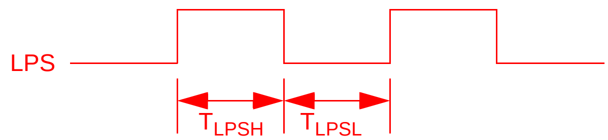


**Figure 5-2 — LPS waveform when Direct is low**

**Table 5-2 — LPS timing parameters**

| Parameter | Description | Unit | Minimum | Maximum |
|---|---|---|---|---|
| $T_{LPSL}$ | LPS low time (when Direct is low) | µs | 0.09 | 2.00 |
| $T_{LPSH}$ | LPS high time (when Direct is low) | µs | 0.09 | 2.00 |
| $T_{LPS\_RESET}$ | Time for PHY to recognize absence of LPS | µs | 2.25 | 2.75 |
| $T_{LPS\_WAIT}$ | Time after PHY removes SClk until link may reassert LPS (when Direct is low) | µs | 10 | |

The link requests the PHY to disable and reset the interface by deasserting LPS. Within 2.25 µs after it deasserts LPS, the link shall place Ctl[0:1] and D[0:*n*] in a high-impedance state and condition LReq according to Direct: if Direct is high, LReq shall be driven zero otherwise it shall be placed in a high-impedance state.

If the PHY does not observe LPS for $T_{LPS\_RESET}$ (as illustrated by figure 5-3), it shall disable and reset the interface. When Direct is TRUE the PHY disables the interface by driving Ctl[0:1], D[0:*n*] and SClk to zero. Otherwise, the PHY disables the interface by placing the Ctl[0:1], D[0:*n*] and SClk signals in a high-impedance state.

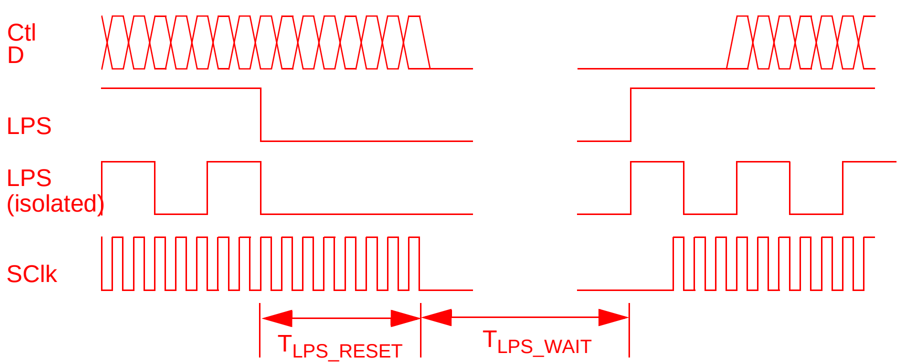


**Figure 5-3 — PHY/link interface reset *via* LPS**

When the PHY/link interface is reset the PHY shall cancel any outstanding bus request or register read request. Although the cancellation of bus requests may affect PHY arbitration states in ways not described in section 7, the PHY's behaviors (as observable from Serial Bus) shall be consistent with that section. For example, the PHY may have initiated arbitration in response to a bus request but reset of the PHY/link interface might cancel the request before it is granted. Appropriate PHY behavior would be either the transmission of a null packet or the removal of the arbitration request before it is granted.

The C code and state machines in section 7 describe the PHY's operation as if the interface to the link is always operational. If the PHY/link interface is reset while the link is transmitting a packet, the PHY shall behave as if the link had signaled *Idle* and terminated the packet. Similarly, any status information generated by the PHY while the interface is disabled shall be discarded and shall not cause a status transfer upon restoration of the interface.

The handshake just described resets the interface when the link deasserts LPS for a minimum of 2.75 µs. Normal operations may be restored if the link reasserts LPS. After observing LPS, the PHY shall resume SClk as soon as possible. Once SClk resumes the PHY and link shall condition their Ctl[0:1] and D[0:*n*] outputs in accordance with table 5-3.

**Table 5-3 — Initialization of the PHY/link interface**

| Device | Direct input | |
|---|---|---|
| | **Low** | **High** |
| PHY | For one and only one of the first six cycles of the resumed SClk, drive Ctl[0:1] and D[0:*n*] to zero and otherwise place them in a high-impedance state. | Continue to drive Ctl[0:1] and D[0:*n*] to zero for the first six cycles of the resumed SClk. |
| Link | For one and only one of the first six cycles of the resumed SClk, drive Ctl[0:1], D[0:*n*] and LReq to zero and otherwise place them in a high-impedance state. | For one and only one of the first six cycles of the resumed SClk, drive Ctl[0:1], D[0:*n*] and LReq to zero; prior to this place them in a high-impedance state. Once these signals have been driven low, return Ctl[0:1] and D[0:*n*] to a high-impedance state but continue to drive LReq low until after the reset completes. |

Upon the seventh and subsequent SClk cycles the PHY shall drive Ctl[0:1] and D[0:*n*] in accordance with its arbitration state machines subject to the following restrictions:

- until the PHY asserts *Receive* on Ctl[0:1] while simultaneously asserting data prefix on D[0:*n*] for at least one SClk cycle, it shall not assert any state other than *Idle* on Ctl[0:1];
- once the PHY indicates data prefix it shall continue to do so until it returns to the idle arbitration state;
- no status information shall be transferred that commences part way through the status bits; and
- no partial packets shall be transferred on D[0:*n*].

The link may examine Ctl[0:1] once it has driven Ctl[0:1], D[0:*n*] and LReq to zero for one cycle subsequent to the availability of SClk. When the link simultaneously observes *Receive* on Ctl[0:1] and data prefix on D[0:*n*] the reset of the PHY/link interface is complete. The link shall not assert LReq until the reset is complete.

## 5.2 Link-on indication

The PHY LinkOn output provides a method to signal the link at times when the link is not active. The link is inactive when either the LPS signal is absent (see clause 5.1) or the PHY register Link_active bit is zero. The characteristics of the LinkOn signal, specified by table 5-4, permit the link to detect LinkOn in the absence of SClk and also permit the signal to cross an optional isolation barrier.

**Table 5-4 — LinkOn timing parameters**

| Description | Unit | Minimum | Maximum |
|---|---|---|---|
| Frequency | MHz | 6.144 ± 100 ppm | |
| Duty cycle | % | 40 | 60 |
| Persistence. Time, measured from the point at which both LPS is active and Link_active is one, after which the PHY shall not signal LinkOn. | ns | | 325.6 |

When either LPS is absent or the PHY register Link-active bit is zero, a PH_EVENT.*indication* of LINK_ON shall cause the assertion of LinkOn. This signal shall persist so long as the logical AND of the LPS signal and Link_active is zero.

At other times (when the link is active), a PH_EVENT.*indication* of LINK_ON shall be communicated to the link by the transfer of the link-on packet that caused the event. The PHY shall not assert LinkOn if the link is already active.

## 6. PHY register map

In addition to the renaming of the PHY register L bit to Link_active, we propose that the bit's power reset value be controllable by a strapping option. This is the same language that was earlier adopted for the contender (C) bit.

**Table 6-1 — PHY register fields for the cable environment**

| Field | Size | Type | Power reset value | Description |
|---|---|---|---|---|
| Link_active | 1 | rw | See description | Link active. Cleared or set by software to control the value of the L bit transmitted in the node's self-ID packet 0, which shall be the logical AND of this bit and LPS active. If hardware implementation-dependent means are not available to configure the power reset value of the Link_active bit, the power reset value shall be one. |

 This is an unapproved standards draft, subject to change 