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FROM: Peter Johansson

TO: IEEE P1394a Working Group

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RE: PHY/Link interface reset and LinkOn behaviors

This document is a joint contribution from Richard Baker, Jerry Hauck, Prashant Kanhere, Jim Skidmore, Colin Whitby-Strevens and myself. We met, some in person, some by telephone, on November 13 and developed these proposals.

The recommendations were subsequently reviewed by an informal group of link and PHY silicon designers (*aka* the PHY dogs), presented to the full working group in Ft. Lauderdale and further reviewed and modified by the PHY designers in Albuquerque, NM.

The proposal takes the form of changes to the first part of section 5 in IEEE P1394a Draft 1.2 followed by two new clauses, Initialization and reset and Link-on indication . There is also a suggestion to modify the description of the Link_active bit in the PHY registers to permit a hardware strapping option for its power reset value.

Of particular interest is the proposal to signal the completion of the PHY/link interface reset. The PHY asserts *Receive* on Ctl[0:1] and data prefix on D[0:*n*] for at least one cycle. The link shall not use the resumed interface (*i.e.*, issue any new requests *via* LReq) until this handshake completes.

In addition, if this proposal is adopted I would make editorial changes throughout section 5 to refer to the interface as either differentiated or unidfferentiated (in place of references to an optional isolation barrier). These changes are recommended because the state of Direct does not unambiguously indicate the presence or absence of an isolation barrier and because Direct is an optional signal on the link.

5. PHY/Link interface

This section standardizes the PHY/link interface previously described in an informative annex of IEEE Std 1394-1995. It specifies the protocol and signal timing. It does not describe specific operation of the PHY except for behavior with respect to this interface.

The interface specified in this section is a scalable method to connect one Serial Bus link chip to one Serial Bus PHY chip. It supports data rates of S25 and S50 in the backplane environment and S100, S200 and S400 in the cable environment. The width of the data bus scales with Serial Bus speed: two signals support speeds up to 100 Mbps while at faster speeds a total of two signals per 100 Mbps are necessary. The clock rate of the signals at this interface remains constant, independent of Serial Bus speed. The interface permits isolation for implementations where it is desirable.

The interface may be used by the link to transmit data, receive data or status, or issue requests. The link makes requests of the PHY *via* the dedicated LReq signal. In response, the PHY may transfer control of the bidirectional signals to the link. At all other times the PHY controls the bidirectional signals.

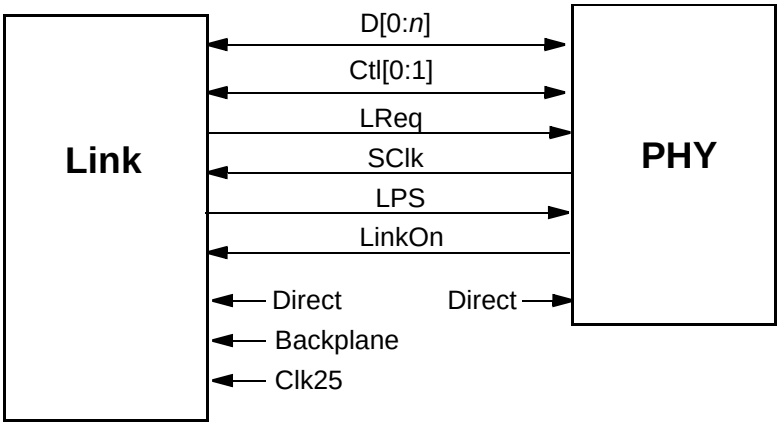

Figure 5-1 — Discrete PHY/link interface

Discrete PHY implementations shall support all of the PHY signals shown in figure 5-1. Discrete link implementations shall support D[0:*n*], Ctl[0:1], LReq and SClk; link support for the other signals is optional. For both PHY and link, the number of data bits implemented, *n*, depends upon the maximum speed supported by the device. The PHY/link interface signals are described in table 5-1.

Table 5-1 — PHY/link signal description

Name	Driven by	Description
D[0:*n*]	Link or PHY	Data
Ctl[0:1]	Link or PHY	Control
LReq	Link	Link request
SClk	PHY	12.288, 24.576 or 49.152 MHz clock (synchronized to the PHY transmit clock)
LPS	Link	Link power status. Indicates that the link is powered and functional
LinkOn	PHY	Occurrence of a link-on event.

Table 5-1 — PHY/link signal description (Continued)

Name	Driven by	Description
Direct	Neither	Set high to disable differentiator outputs for the Ctl[0:1], D[0:*n*] and LReq signals. ~~Set high to indicate a direct connection or low to indicate an isolation barrier between the link and PHY.~~
Backplane	Neither	Set high if backplane PHY
Clk25	Neither	Meaningful only if Backplane is high. Set high to indicate a 24.576 MHz SClk; otherwise 12.288 MHz.

Data is transferred between the PHY and link on D[0:*n*]. The implemented width of D[0:*n*] depends on the maximum speed of the ~~connected PHY~~ device: 2 bits for S100 or slower, 4 bits for S200 and 8 bits for S400. At S100 or slower, packet data is transferred on D[0:1], at S200 on D[0:3] and at S400 on D[0:7]. Implemented but unused D[0:*n*] signals shall be driven low by the device that has control of the interface.

~~The Ctl bus signals control information and is two bits wide.~~

The LReq signal is used by the link to request access to Serial Bus for packet transmission, to read or write PHY registers or to control arbitration acceleration.

The presence of a stable SClk signal generated by the PHY is necessary for the PHY/link interface to be operational. When SClk is not shown in the timing diagrams in this section, each Ctl[0:1], D[0:*n*] or LReq bit cell represents a single clock sample time. The specific timing relationships ~~clock-to-data timing relationships~~ are described in clauses 5.6.2 and 5.6.3.

The LPS signal may be used by the link to disable SClk or reset the interface, as specified in clause 5.1.

The LinkOn signal permits the PHY to indicate an interrupt to the link when either LPS is logically false or the PHY register Link_active bit is zero. The details are specified in clause 5.2.

The Direct input controls digital differentiators on the D[0:*n*], Ctl[0:1]~~, SClk, LPS, LinkOn~~ and LReq signals. When set high it shall disable differentiator outputs on these signals (which shall be otherwise enabled). In the case that the link does not implement Direct, the link shall be configured so that output on these signals, differentiated or not, conforms to the value of Direct provided to the PHY.

NOTE—Differentiators may be required when the PHY and link are connected through an optional isolation barrier. A digital differentiator drives its output signal for one clock period whenever the input signal changes, but places the output signal in a high-impedance state so long as the input signal remains constant. Figure 5-2 illustrates this signal transformation.

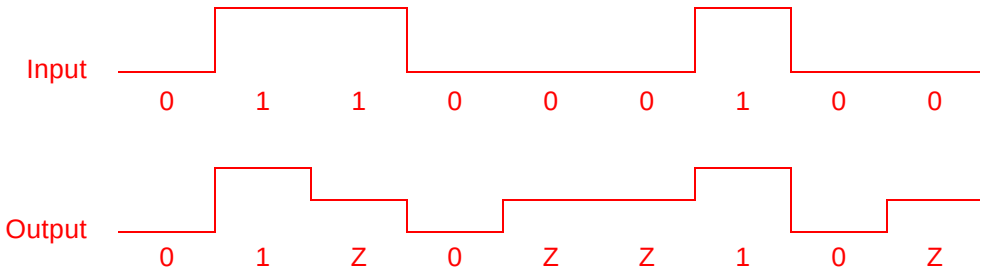

Figure 5-2 — Digital differentiator signal transformation

When a backplane PHY is connected to a link the Backplane input shall be strapped high. The Clk25 input is meaningful only to indicate the SClk frequency generated by a backplane PHY. In the backplane environment, data transfers use D[0:1]. SClk is used to clock the transfers at either 12.288 MHz (for TTL applications) or 24.576 MHz (for BTL and ECL applications). This yields PHY data rates at the backplane of S25 and S50, respectively.

~~Whenever control is transferred between the PHY and the link, the side relinquishing control always drives the control and data buses to logic zero levels for one clock before placing those signals in a high-impedance state. An additional clock with zero on the control and data signals is necessary for the link when it is transferring control to the PHY without a *hold* request. This is necessary to ensure that an optional differentiator circuit can operate properly.~~

5.1 Initialization and reset

The LPS input requests the PHY to disable or enable the PHY/link interface. The output characteristics of LPS, if provided by the link, depend upon the interface mode, differentiated or undifferentiated. When the interface mode is differentiated, LPS shall be a pulsed output while logically asserted. The characteristics of LPS are specified by figure 5-3 and table 5-2.

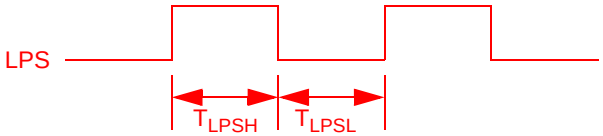

Figure 5-3 — LPS waveform when differentiated

Table 5-2 — LPS timing parameters

Parameter	Description	Unit	Minimum	Maximum
T_{LPSL}	LPS low time (when pulsed)	µs	0.09	1.00
T_{LPSH}	LPS high time (when pulsed)	µs	0.09	1.00
T_{LPS_RESET}	Time for PHY to recognize LPS logically deasserted	µs	1.2	2.75
T_{LPS_WAIT}	Time after PHY removes SClk until link may reassert LPS (when differentiated)	µs	10	

The link requests the PHY to disable and reset the interface by deasserting LPS. Within 1.2 µs after it deasserts LPS, the link shall place Ctl[0:1] and D[0:*n*] in a high-impedance state and condition LReq according to the interface mode: if undifferentiated, LReq shall be driven zero otherwise it shall be placed in a high-impedance state.

If the PHY observes LPS logically deasserted for T_{LPS_RESET}, it shall disable and reset the interface. The voltage levels show in figure 5-4 for Ctl[0:1], D[0:*n*], LReq and SClk while LPS is logically deasserted are accurate only for a undifferentiated interface, but the timing relationships remain accurate for both modes. When the interface is undifferentiated, the PHY disables the interface by driving Ctl[0:1], D[0:*n*] and SClk to zero. Otherwise, the PHY disables the interface by placing the Ctl[0:1], D[0:*n*] and SClk signals in a high-impedance state.

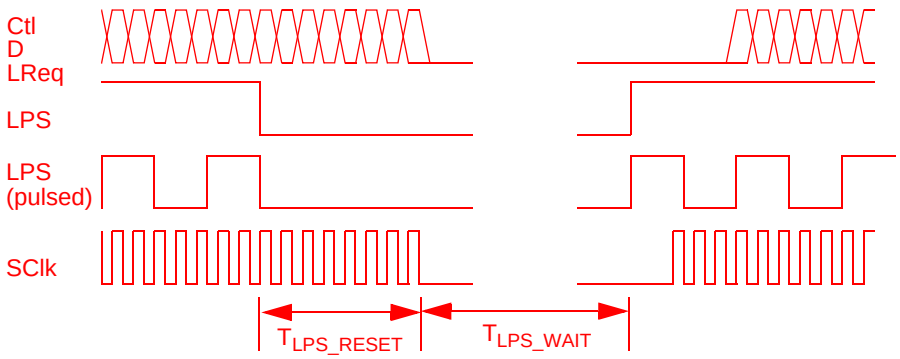

Figure 5-4 — PHY/link interface reset *via* LPS

When the PHY/link interface is reset the PHY shall cancel any outstanding bus request or register read request. Although the cancellation of bus requests may affect PHY arbitration states in ways not described in section 7, the PHY's behaviors (as observable from Serial Bus) shall be consistent with that section. For example, the PHY may have initiated arbitration in response to a bus request but reset of the PHY/link interface might cancel the request before it is granted. Appropriate PHY behavior would be either the transmission of a null packet or the removal of the arbitration request before it is granted.

The C code and state machines in section 7 describe the PHY's operation as if the interface to the link is always operational. If the PHY/link interface is reset while the link is transmitting a packet, the PHY shall behave as if the link had signaled *Idle* and terminated the packet. Similarly, any status information generated by the PHY while the interface is disabled shall be discarded and shall not cause a status transfer upon restoration of the interface.

The handshake just described resets the interface when the link deasserts LPS for a minimum of 2.75 µs. Normal operations may be restored if the link reasserts LPS. After observing LPS, the PHY shall resume SClk as soon as possible. Once SClk resumes the PHY and link shall condition their Ctl[0:1] and D[0:*n*] outputs in accordance with table 5-3.

Table 5-3 — Initialization of the PHY/link interface

Device	Interface mode	
	Differentiated	Undifferentiated
PHY	For one and only one of the first six cycles of the resumed SClk, drive Ctl[0:1] and D[0:*n*] to zero and otherwise, for these cycles and the seventh, place them in a high-impedance state.	Continue to drive Ctl[0:1] and D[0:*n*] to zero for the first seven cycles of the resumed SClk.
Link	For one and only one of the first six cycles of the resumed SClk, drive Ctl[0:1], D[0:*n*] and LReq to zero and otherwise place them in a high-impedance state.	For one and only one of the first six cycles of the resumed SClk, drive Ctl[0:1], D[0:*n*] and LReq to zero; prior to this place them in a high-impedance state. Once these signals have been driven low, return Ctl[0:1] and D[0:*n*] to a high-impedance state but continue to drive LReq low until after the reset completes.

Upon the eighth and subsequent SClk cycles the PHY shall drive Ctl[0:1] and D[0:*n*] as follows:

- if the PHY is in the idle arbitration state, it shall assert *Receive* on Ctl[0:1] while simultaneously asserting data prefix on D[0:*n*] for at least one SClk cycle;
- until the PHY indicates data prefix as described above, it shall not assert any state other than *Idle* on Ctl[0:1];
- once the PHY indicates data prefix it shall continue to do so until it is in the idle arbitration state, at which time it shall assert *Idle* on Ctl[0:1];
- no status information shall be transferred that commences part way through the status bits; and
- no partial packets shall be transferred on D[0:*n*].

The link may examine Ctl[0:1] once it has driven Ctl[0:1], D[0:*n*] and LReq to zero for one cycle subsequent to the availability of SClk. When the link simultaneously observes *Receive* on Ctl[0:1] and data prefix on D[0:*n*] the reset of the PHY/link interface is complete. The link shall not assert LReq until the reset is complete.

5.2 Link-on indication

The PHY LinkOn output provides a method to signal the link at times when the link is not active. The link is inactive when either the LPS signal is logically deasserted (see clause 5.1) or the PHY register Link_active bit is zero. The characteristics of the LinkOn signal, specified by table 5-4, permit the link to detect LinkOn in the absence of SClk and also permit the signal to cross an optional isolation barrier.

Table 5-4 — LinkOn timing parameters

Description	Unit	Minimum	Maximum
Frequency	MHz	4	8
Duty cycle	%	40	60
Persistence. Time, measured from the point at which both LPS is active and Link_active is one, after which the PHY shall not signal LinkOn.	ns		500

When either LPS is logically false or the PHY register Link-active bit is zero, a PH_EVENT.*indication* of LINK_ON shall cause the assertion of LinkOn. This signal shall persist so long as the logical AND of the LPS signal and Link_active is zero.

At other times (when the link is active), a PH_EVENT.*indication* of LINK_ON shall be communicated to the link by the transfer of the link-on packet that caused the event. The PHY shall not assert LinkOn if the link is already active.

5.4 Transmit

A paragraph previously located in the introductory material of section 5 is moved to the clause that describes transmit. This rendered an existing note redundant, which is deleted. The changes proposed by Steve Finch in Ft. Lauderdale are also shown below. The remainder of current clause 5.4 (including figure 5-6, not reproduced here) in P1394a Draft 1.2 remains unchanged.

When the link requests access to Serial Bus through the LReq signal, the PHY arbitrates for access to Serial Bus. If the PHY wins the arbitration, it grants the bus to the link by asserting *grant* on Ctl[0:1] for one SClk cycle, followed by *idle* for one cycle. After observing *grant* followed by *idle* on Ctl[0:1], the link takes control of the interface by asserting *idle*, *hold* or *transmit* on Ctl[0:1] one cycle after sampling *idle* from the PHY. The link should assert *idle* for one cycle before changing the state of Ctl[0:1] to either *hold* or *transmit* but shall not assert *idle* for more than one cycle. PHY implementations shall tolerate *idle* for one cycle prior to *hold* or *transmit*. The link asserts *hold* to keep ownership of the bus while preparing data. The PHY asserts DATA_PREFIX on Serial Bus during this time. When it is ready to begin transmitting a packet, the link asserts *transmit* on Ctl[0:1] along with the first bits of the packet. After sending the last bits of the packet, the link asserts either *idle* or *hold* on Ctl[0:1] for one cycle and then it asserts *idle* for one additional cycle before placing those signals in a high-impedance state.

Whenever control of the bidirectional signals is transferred between the PHY and link, the device relinquishing control shall drive Ctl[0:1] and D[0:*n*] to logic zero levels for one clock before releasing the interface. This permits both devices to act upon registered versions of the interface signals while allowing the new owner a clock cycle in which to sample and respond. Note that when the link transfers control to the PHY without a *Hold* request, an additional clock with logic zero on the control and data signals is necessary so as not to place the signal lines in a high impedance state before the PHY takes control.

An assertion of *hold* after the last bits of a packet indicates to the PHY that the link needs to send another packet without releasing the bus. This function is used by the link to concatenate a packet after an acknowledge or to concatenate isochronous packets. With this assertion of *hold* the link simultaneously signals the speed of the next packet on the data lines, as encoded by table 5-16. Once *hold* is asserted, the PHY waits a MIN_PACKET_SEPARATION time and then asserts *grant* as before. After observing *grant* on Ctl[0:1], the link resumes control of the interface by asserting *idle*, *hold* or *transmit* on Ctl[0:1]. The link should assert *idle* for one SClk cycle, but shall not assert *idle* for more than one cycle, before changing Ctl[0:1] to *hold* or *transmit*. The link shall ensure that the time from when it asserts *hold* on Ctl[0:1] (at the end of a packet) to when it asserts *transmit* on Ctl[0:1] (and starts to provide data for the concatenated packet on D[0:*n*]) does not exceed MAX_BUS_HOLD less the delay between the PHY's transmission of TX_DATA_PREFIX and its assertion of *grant* on Ctl[0:1].

The link may transmit concatenated packets at a different speeds, with one exception: the link shall not concatenate an S100 packet after any packet of a higher speed. When the link wishes to send an S100 packet after any packet of a higher speed, it shall make a separate isochronous request.

NOTE—If the multi-speed capabilities of the PHY have not been enabled (see clause 6.1), all concatenated packets shall be transmitted at the speed originally specified as part of the bus request. This requirement provides for backward compatibility when a PHY compliant with this specification is interfaced to a link that is not aware of the necessity to signal speed for each packet.

As noted above, when the link has finished sending the last packet, it releases the bus by asserting *idle* on Ctl[0:1] for two SClk cycles. The PHY begins asserting *idle* on Ctl[0:1] one cycle after sampling *idle* from the link.

~~NOTE—Whenever the link and PHY exchange ownership of D[0:*n*] and Ctl[0:1], the entity relinquishing control shall refrain from sampling the interface for one cycle. This permits both link and PHY to act upon registered versions of the interface signals and also permits the new owner one cycle in which to sample and respond.~~

NOTE—The timings for both a single and a concatenated packet transmit operation are illustrated in figure 5-6. In the diagram, D0 through D_n are the data symbols of the packet, SP represents the speed code for the packet (encoded according to the values specified in table 5-16) and ZZ represents high impedance state. The link should assert the signals indicated by the shaded SClk cycles (this may be necessary in the presence of an isolation barrier).

6. PHY register map

In addition to the renaming of the PHY register L bit to Link_active, we propose that the bit s power reset value be controllable by a strapping option. This is the same language that was earlier adopted for the Contender bit.

Table 6-1 — PHY register fields for the cable environment

Field	Size	Type	Power reset value	Description
Link_active	1	rw	See description	Link active. Cleared or set by software to control the value of the L bit transmitted in the node's self-ID packet 0, which shall be the logical AND of this bit and LPS active. If hardware implementation-dependent means are not available to configure the power reset value of the Link_active bit, the power reset value shall be one.