FIFO Centering Proposal

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Discussion

In a S400 implementation, there are eight dribble bits. The maximum packet length is 4096 bytes. At clock frequencies specified with a tolerance of +/- 100 ppm, this equates to a maximum excess of transmit over receive or receive over transmit of 6.something bits, round up to 7. At S200, its 3.something, round up to 4.

To avoid the possibility of an early underflow detection (see `rx_bit` in Table 7-15), the FIFO has to be stocked up with enough bits to hold the dribble bits, plus enough bits to allow for maximum transmit over receive, i.e. 15 bits. If the FIFO is stocked up with 15 bits, then there is also the possibility that the there is a maximum excess of receive over transmit of 7 bits, and so the FIFO_DEPTH has to be at least 22 bits to avoid the possibility of overflow.

In summary at S400, we have to wait for 8 dribble bits, plus 7 bits for clock variation
At S200, its 4+4. At S100, its 2+2

At S400, the buffer has to be able to hold 8 dribble bits, plus 14 bits for clock variation i.e. 22.
At S200, its 4+8, i.e. 12. At S100, its 2+4, i.e. 6

Everything is much easier if your round up the clock frequency variation bits for S400 to 8!

The proposal (below) also has the benefit of clarifying one aspect of the PHY_DELAY debate, and that is that the PHY delay applies to the first bit of the packet. The relative clock frequency differences means that the last bit of a packet can be delayed 8 bit times less than the minimum PHY delay, or 8 bit times more than the maximum PHY delay (this is at S400, in fact the time is always 20ns).

Proposal

Replace:-

```
const int FIFO_DEPTH = 8; // IMPLEMENTATION-DEPENDENT!

for (i = 0; i < FIFO_DEPTH/2 - 1; i++)
wait_event(PHY_CLOCK_indication); // Make sure FIFO is centered
```

by:-

```
const int FIFO_DEPTH = ?; // at least 6 bits for S100 PHY,
                          // 12 for S200 PHY, 24 for S400 PHY


for (i = 0; i < rx_dribble_bits * 2 - 1; i++)
wait_event(PHY_CLOCK_indications); // buffer enough bits to allow for max
                                   // difference in clock freqencies (same
                                   // value as dribble_bits)
                                   // and for dribble bits
```

Also noted in passing: CONCATENATION_PREFIX_TIME is not defined in the list of PHY constants