P1394a
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FIFO Centering

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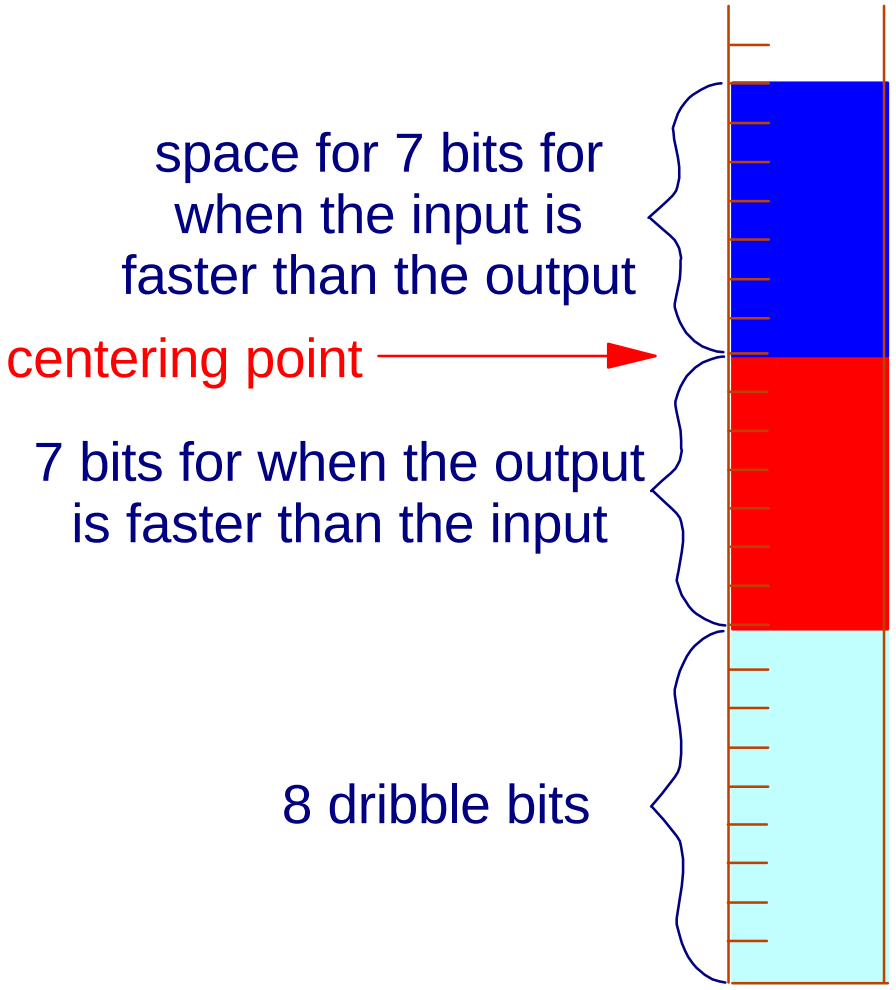
Summary

- FIFO (elastic) buffer required in the receiving PHY to compensate for clock frequency differences between sender and receiver
- Current draft is wrong
  - × wrong (minimum) buffer size
  - × wrong FIFO centering algorithm
- Dribble bits need to be taken into account
  - "Empty" test is when there are only dribble bits left in the FIFO
    - ✓ test made on count of bits
    - ✓ need to ensure that there are always more than "dribble bits" in the buffer until the end of packet
- Centering algorithm needs to allow first for dribble bits, and then for clock differences for max packet size
  - both are speed dependent

Details

- Dribble bits
  - 2 for S100, 4 for S200, 8 for S400
- Excess of send over receive or receive over send
  - max packet is 4096 bytes
  - max clock disparity is 200 ppm (each clock is +/- 100 ppm)
  - excess calculates to
    - ✓ S400: 6.5536 bits - round up to 7
    - ✓ S200: 3.2768 bits - round up to 4
    - ✓ S100: 1.6384 bits - round up to 2
- FIFO size for S400 is min 22 bits
  - round up to 24 for ease of handling
  - excess then happens to equal `rx_dribble_bits`



Proposed changes

Replace:-

```
const int FIFO_DEPTH = 8; // IMPLEMENTATION-DEPENDENT!

for (i = 0; i < FIFO_DEPTH/2 - 1; i++)
wait_event(PHY_CLOCK_indication); // Make sure FIFO is centered
```

by:-

```
const int FIFO_DEPTH = ?; // at least 6 bits for S100 PHY,
                          // 12 for S200 PHY, 24 for S400 PHY


for (i = 0; i < rx_dribble_bits * 2 - 1; i++)
wait_event(PHY_CLOCK_indications); // buffer enough bits to allow for max
                                   // difference in clock freqencies (same
                                   // value as dribble_bits)
                                   // and for dribble bits
```