Continuous SClk Proposal

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1. Summary

A significant class of 1394 applications can save costs by operating the link, transaction and application layers within the single clock domain provided by the PHY's SClk. Three technical changes are required to permit this:-

1. Keep SClk running during a reset of the PHY/Link interface (but not during disable)
2. Provide SClk with LinkOn
3. Tighten up the duty cycle for SClk

We propose that the costs of these changes is minimal, and worth paying to allow this potential system cost saving for a significant class of applications.
The proposal also clarifies how the interface is initialized on power reset.

2. Proposed changes (c/f PHY/Link interface report also being submitted)

2.1 SClk specification (Table 5-18)

The duty cycle is modified to 47.5%/52.5%.
This increases the effective clock period for the Link/Application from 8ns to 9.5ns.

2.2 Initialization and reset (Clause 5.1)

Modify the specification of T_{LPS_WAIT} to "LPS deassertion time".
Modify the minimum value for T_{LPS_WAIT} to 12.5 us.
Modify the text of the second and third paragraphs as follows:-

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The Link requests the PHY to ~~disable and~~ reset and possibly disable the interface by deasserting LPS. Within 2.25 us of the time it deasserts LPS, the Link shall place Ctl[0:1], and D[0:n] in a high impedance state and condition LReq according to Direct: if Direct is present and low, LReq shall be placed in a high impedance state, otherwise it shall be driven low."

The Link requests the PHY to reset the interface by deasserting LPS for a minimum of T_{LPS_WAIT} and for a maximum of $T_{LPS\_WAIT} + T_{LPS\_RESET}$. The Link requests the PHY to disable the interface by deasserting LPS for longer than $2*(T_{LPS\_WAIT} + T_{LPS\_RESET})$.

The interface is reenabled either by the Link reasserting LPS, possibly in response to a LinkOn signal from the PHY.

If the PHY observes LPS deasserted for T_{LPS_RESET} (as illustrated by figure 5-3), it shall ~~disable and~~ reset the interface. If the PHY observes LPS deasserted for $T_{LPS\_RESET} + 2*T_{LPS\_WAIT}$ it shall disable the interface.

When Direct is TRUE the PHY resets the interface by driving Ctl[0:1] and D[0:n] ~~and SClk~~ to zero. Otherwise, the PHY resets the interface by placing the Ctl[0:1] and D[0:n] ~~and SClk~~ signals in a high-impedance state.

When Direct is TRUE the PHY disables the (already reset) interface by driving SClk to zero. Otherwise, the PHY disables the interface by placing the SClk signals in a high-impedance state.

Modify Figure 5-3 to show SClk present during PHY/Link interface reset, and to show min/max

timings (T_{LPS_WAIT} starting from when LPS is deasserted).

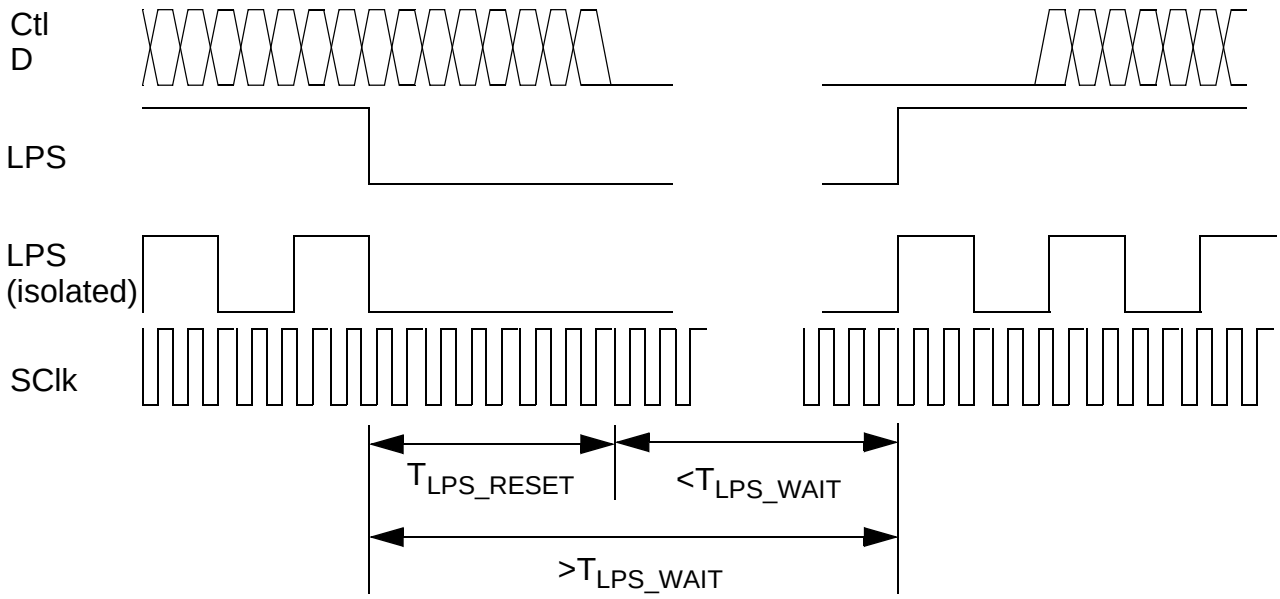

Figure 5-3 - PHY-Link reset timing

Add a new figure to show PHY-Link disable timing

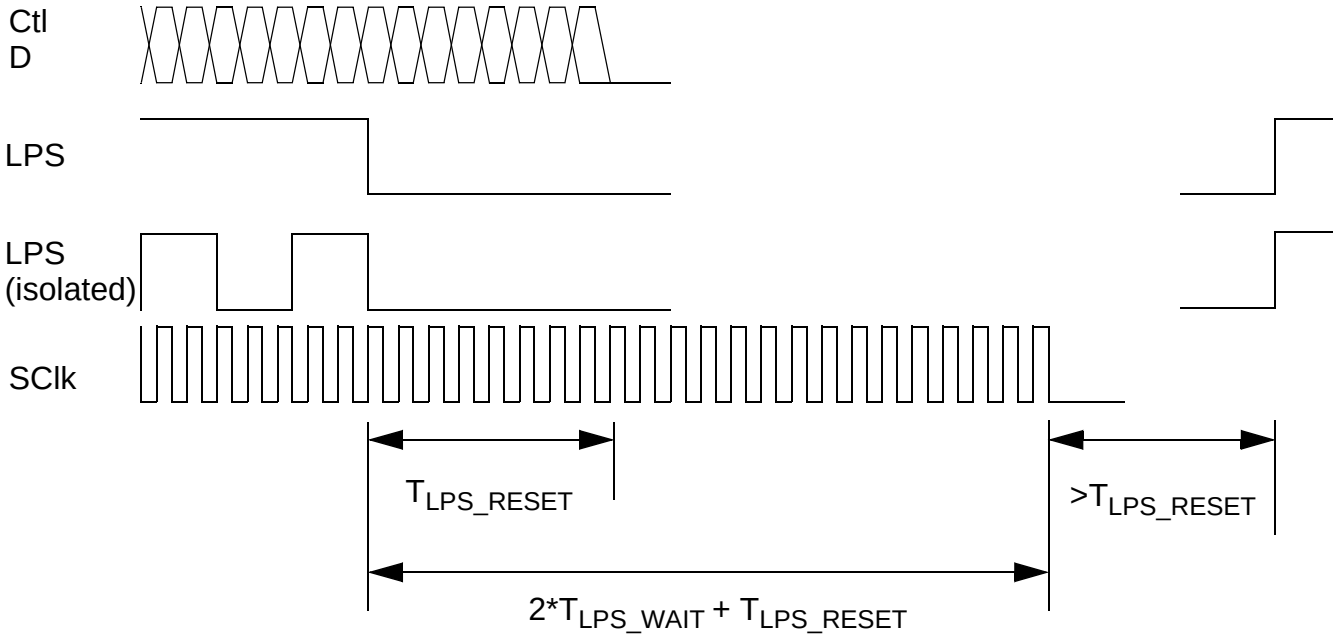

Figure 5-nn - PHY-Link disable timing

Modify the paragraphs describing resumption as follows:-

The handshake just described resets the interface when the link deasserts LPS for a minimum of 2.75 µs, and disables it when the Link deasserts LPS for a minimum of 27.5 µs. Normal operations

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may be restored if the link reasserts LPS. After observing LPS, the PHY shall resume SClk (if necessary) as soon as possible, and then the PHY and the Link shall then initialize the interface as described below.

5.1.1 Interface Initialization

Following a power reset, the PHY shall provide SClk for a period of 2 * T_{LPS_WAIT} and then check for the presence of the LPS signal. If the LPS signal is not asserted then the PHY shall reset and possibly disable the interface as if the LPS signal was deasserted at that moment, as described above.

Once SClk is provided ~~resumes~~ the PHY and link shall condition their Ctl[0:1] and D[0:n] outputs in accordance with table 5-3. In this table, SClk cycles are counted from the later of (i) the time at which SClk is provided, (ii) the time the PHY detects the presence of LPS.

Delete the phrase “the resumed” in Table 5-3 (three occurrences).

Editorial - start clause 5.1 with the description of the initialization of this interface (suggested as Cluase 5.1 above), and then describe reset and disable.

2.3 LinkOn (Clause 5.2)

Modify the first sentence of the LinkOn description:- “The characteristics of the LinkOn signal, Sepcified by table 5-4, permit the link to detect LinkOn when the Link is not active ~~in the absence of SClk~~ and also permit the signal to cross an optional isolation barrier.

Adjust the second and third sentences:- “. . shall cause the assertion of LinkOn, and shall cause the PHY to provide SClk as defined in 5.1.1. The LinkOn ~~This~~ signal shall persist . . .”

3. Further discussion

It should be observed that, as the link/application layer is dependent on the PHY’s clock, the class of devices able to benefit from this change does not include devices in which the link/application is required to run whilst the PHY core is suspended, or the PHY is otherwise not powered. Such devices will require a separate clock to be provided to the link/application.
Note that care has been taken to ensure that “single clock domain” devices are provided with SClk from the PHY before having to assert LPS, and so are able to derive LPS as an oscillating signal from SClk.

Some concern has been expressed as to the advisability of driving SClk into a device which may not be powered. Firstly, I would observe that exactly the same problem happens with LinkOn, and indeed in reverse with LPS. Secondly, I understand that devices commonly have protection circuitry to avoid such problems. But if it is remains a concern, then the proposed behaviour can be controlled via a strap-option status bit.