Continuous SClk Proposal

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1. Summary

A significant class of 1394 applications can save costs by operating the link, transaction and application layers within the single clock domain provided by the PHY's SClk. Three technical changes are required to permit this:-

1. Tighten up the duty cycle for SClk
2. The addition of an option to provide a LinkOn event on power-on reset
3. Keep SClk running during a reset of the PHY/Link interface (but not during suspend)

We suggest that the costs of these changes is minimal, and worth paying to allow this potential system cost saving for a significant class of applications.

The proposal also clarifies how the interface is initialized on power reset.

2. Proposed changes (c/f PHY/Link interface report 97-079r1)

2.1 SClk specification (Table 5-18)

The duty cycle is modified to 47.5%/52.5%.

This increases the effective clock period for the Link/Application from 8ns to 9.5ns.

2.2 LinkOn on power reset

On a power reset and in the absence of LPS the PHY generates a LinkOn event. This is provided by altering the initial value of the Port_status register bit to 1. If there is concern that this should be optional, then the following is added to the description of Port-Status If hardware implementation-dependent means are not available to configure the power reset value of the Port_status bit, the power reset value shall be one.

2.3 Initialization and reset (Clause 5.1)

Update table 5-2

Table 5.2: LPS timing parameters

Parameter	Description	Unit	Minimum	Maximum
T_{LPSL}	LPS low time (when differentiated)	us	0.09	1.00
T_{LPSH}	LPS high time (when differentiated)	us	0.09	1.00

Table 5.2: LPS timing parameters

Parameter	Description	Unit	Minimum	Maximum
T_{LPS_RESET}	Time for PHY to recognise absence of LPS signal for PHY/Link interface reset	us	1.2	2.75
$T_{LPS\_RESET\_WAIT}$	Time that Link holds LPS low for PHY/Link interface reset (when not differentiated)	us	3	12.75
$T_{LPS\_RESET\_WAIT}$	Time that Link holds LPS low for PHY/Link interface reset (when differentiated)	us	10	12.75
$T_{LPS\_SUSPEND\_WAIT}$	Time that Link holds LPS low for PHY/Link interface suspend	us	25.5	

Modify the text of the second and third paragraphs as follows:-

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The Link requests the PHY to ~~disable and~~ reset and possibly suspend the interface by deasserting LPS. Within 1.2 us after it deasserts LPS, the Link shall place Ctl[0:1], and D[0:n] in a high impedance state and condition LReq according to the interface mode: if differentiated, LReq shall be placed in a high impedance state, otherwise it shall be driven to zero. The Link completes the reset by reasserting LPS after waiting for $T_{LPS\_RESET\_WAIT}$ and then follows the initialization procedure as specified in 5.1.1. below.

The Link requests the PHY to suspend the interface by deasserting LPS for a minimum of $T_{LPS\_SUSPEND\_WAIT}$. The interface is re-enabled by the Link reasserting LPS at any time after it sees the PHY withdraw SClk, and then following the initialization procedure as specified in 5.1.1 below.

Note: typically the Link will re-enable the interface in response to a LinkOn signal from the PHY.

If the PHY observes LPS deasserted for T_{LPS_RESET} (as illustrated by figure 5-3), it shall ~~disable and~~ reset the interface. If the PHY observes LPS deasserted for $T_{LPS\_SUSPEND\_WAIT}$ it shall suspend the interface.

When the interface is differentiated, the PHY resets the interface by placing the Ctl[0:1] and D[0:n] ~~and SClk~~ signals in a high-impedance state. Otherwise, the PHY resets the interface by driving Ctl[0:1] and D[0:n] ~~and SClk~~ to zero.

When the interface is differentiated, the PHY suspends the (already reset) interface by placing the SClk signal in a high-impedance state. Otherwise, the PHY suspends the interface by driving SClk to zero.

Modify Figure 5-3 to show SClk present during PHY/Link interface reset, and to show min./max timings (T_{LPS_WAIT} starting from when LPS is deasserted).

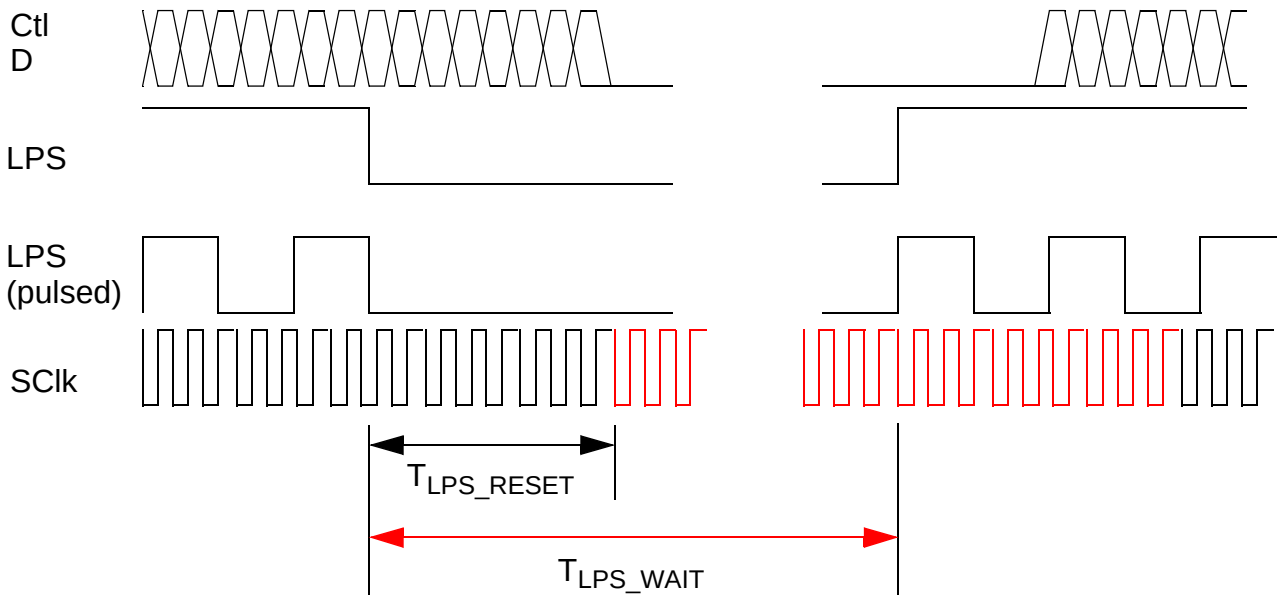

Figure 5-3 - PHY-Link reset timing

Add a new figure to show PHY-Link suspend timing

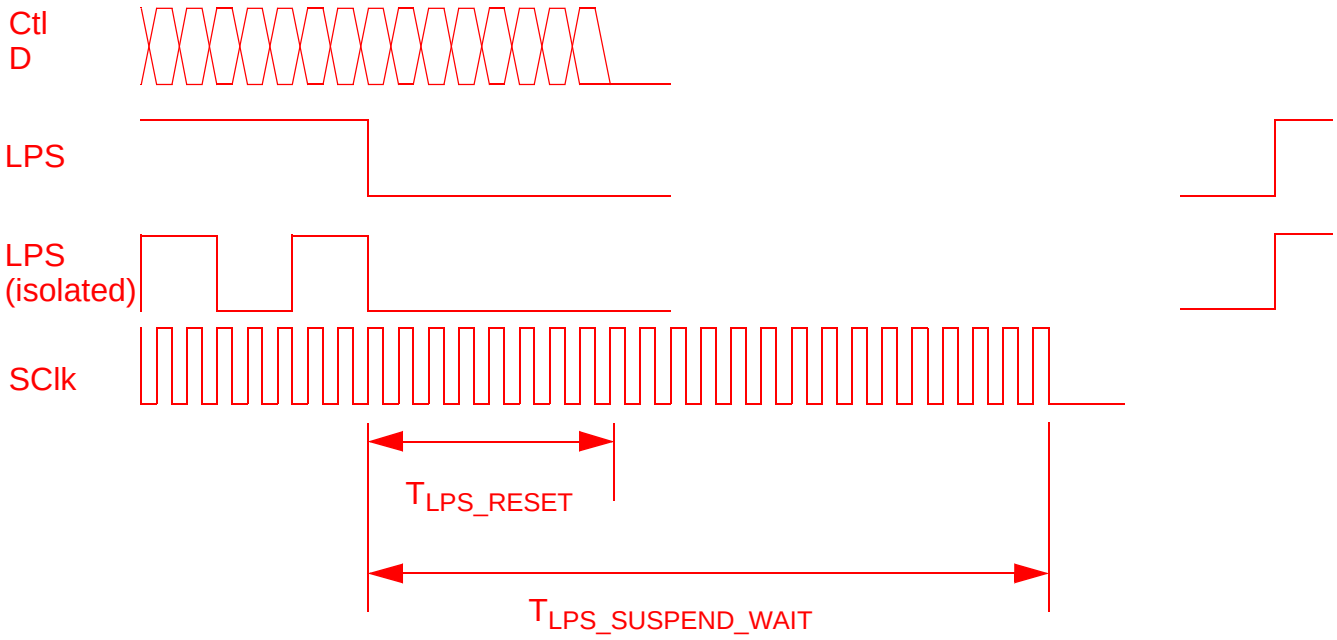

Figure 5-nn - PHY-Link suspend timing

Modify the paragraphs describing resumption as follows:-

The handshake just described resets the interface when the link deasserts LPS for a minimum of 2.75 µs, and suspends it when the Link deasserts LPS for a minimum of 25.5 µs. Normal operation is restored when the link reasserts LPS (as described in 5.1.1 below). ~~After observing LPS, the PHY shall resume SClk as soon as possible.~~

5.1.1 Interface Initialization

Following a power reset, the PHY and the link initialize the interface in the suspend state, as described above.

Following a power reset or a PHY link interface reset, the link continues the initialization of the interface by asserting LPS. After observing LPS, the PHY shall resume SClk (if necessary) within 2 SClk periods if it is asserting LinkOn, and otherwise within TBD (???1 millisecond??? - the limit needed for suspend/resume to work) otherwise. If in differentiated mode, the PHY shall resume SClk by driving it low for half a SClk period.

Once SClk is provided ~~resumes~~ the PHY and link shall condition their Ctl[0:1] and D[0:n] outputs in accordance with table 5-3. In this table, the link counts SClk cycles from the later of (i) the time it detects SClk and (ii) the time it provides LPS, and the PHY counts SClk cycles from the later of (i) the time it provides SClk and (ii) the time it detects the presence of LPS.

Delete the phrase “the resumed” in Table 5-3 (four places)

Editorial - start clause 5.1 with the description of the initialization of this interface (suggested as Clause 5.1 above), and then describe reset and suspend.

3. Further discussion

It should be observed that, as the link/application layer is dependent on the PHY’s clock, the class of devices able to benefit from this change does not include devices in which the link/application is required to run whilst the PHY core is suspended, or the PHY is otherwise not powered. Such devices will require a separate clock to be provided to the link/application.

However, the original proposal was also limited to applications where the only method of bringing the PHY out of suspend was an event on the serial bus. This revised proposal removes this limitation - an external application-related event may now result in the assertion of LPS, which will bring the PHY out of suspend and then the Link out of suspend (subject to final details of the Suspend/Resume proposal).

This proposed specification for initialization of the interface operates in various possible scenarios as follows:-

1) Power on reset, link provides an immediate continuous LPS signal

The PHY will not generate a LinkOn. It provides SClk when it is able to - i.e. when its internal clocks are nice and stable. The PHY and the Link count the interface reset cycles by reference to

the first edge of SClk sent by the PHY.

2) Power on reset, link does not provide LPS

The PHY will wait until its internal clocks are nice and stable, and then will provide a LinkOn. The Link (or the Link power management logic) will at some time later provide LPS. On detecting the rising edge of LPS, the PHY will provide SClk within two cycles. The PHY and the Link count the interface reset cycles by reference to the first edge of SClk sent by the PHY.

3) Resumption from Suspend initiated by the Link (Link provides LPS)

The PHY gets its clocks going if necessary, and then provides SClk. The PHY and the Link count the interface reset cycles by reference to the first edge of SClk sent by the PHY

4) Resumption from Suspend initiated by the PHY (Link is not providing LPS)

The PHY will wait until its internal clocks are nice and stable, and then will provide a LinkOn. The Link (or the Link power management logic) will at some time later provide LPS. On detecting the rising edge of LPS, the PHY will provide SClk within two cycles. The PHY and the Link count the interface reset cycles by reference to the first edge of SClk sent by the PHY.

5) PHY Link reset

The Link reasserts LPS between 3 and 12.5 us after deasserting it. SClk runs continuously. The PHY and the link count the interface reset cycles by reference to the first SClk cycle sent by the PHY after the link asserts LPS. Note that the Link may count from one SClk cycle earlier than the PHY. This has no effect on correct functioning of the interface, as it will appear to the Link as if the PHY has completed the reset of the interface one cycle later.