Continuous SClk Proposal

Colin Whitby-Strevens
ST
P1394a Houston January 1998

1. Summary

A significant class of 1394 applications can save costs by operating the link, transaction and application layers within the single clock domain provided by the PHY's SClk. Two technical changes are required to facilitate this:-

1. Tighten up the duty cycle for SClk
2. Keep SClk running during a reset of the PHY/Link interface (but not during suspend)

We suggest that the costs of these changes is minimal, and worth paying to allow this potential system cost saving for a significant class of applications.

As an editorial change, we propose using the term *suspend* instead of *disable* - in order to be consistent with the terminology used in the Suspend/Resume proposal for the treatment of PHY ports. The "suspended" PHY/link interface can be brought out of suspend by actions either by the PHY or by the link. The term disable should be reserved for the more dramatic mode (which does not apply here) when a port ignores all external signals.

The proposal also clarifies how the interface is initialized on power reset. This is consistent with the proposal made in the PHYDOGs meeting in Albuquerque.

2. Proposed changes (c/f P1394a Draft 1.3)

2.1 SClk specification (Table 5-18)

The duty cycle is modified to 45%/55%.

This increases the effective clock period for the Link/Application from 8ns to 9ns.

2.2 Initialization and reset (Clause 5.1)

Table 5-2 is updated to provide two timing constants, one for reset and a longer one for suspend. Also this proposal allows a more efficient time for reset in the non-pulsed case.

Table 5.2: LPS timing parameters

Parameter	Description	Unit	Minimum	Maximum
T_{LPSL}	LPS low time (when pulsed)	µs	0.09	1.00
T_{LPSH}	LPS high time (when pulsed)	µs	0.09	1.00
T_{LPS_RESET}	Time for PHY to recognize LPS logically deasserted	µs	1.2	2.75

Table 5.2: LPS timing parameters

Parameter	Description	Unit	Minimum	Maximum
$T_{LPS\_RESET\_WAIT}$	Time that Link holds LPS low for PHY/Link interface reset (when not pulsed)	µs	3	12.75
$T_{LPS\_RESET\_WAIT}$	Time that Link holds LPS low for PHY/Link interface reset (when pulsed)	µs	10	12.75
$T_{LPS\_SUSPEND\_WAIT}$	Time that Link holds LPS low for PHY/Link interface suspend	µs	25.5	

Modify the text of the second and third paragraphs of Clause 5.1 as follows:-

---

The Link requests the PHY to ~~disable and~~ reset and possibly suspend the interface by deasserting LPS. Within 1.2 µs after it deasserts LPS, the Link shall place Ctl[0:1], and D[0:n] in a high impedance state and condition LReq according to the interface mode: if undifferentiated, LReq shall be driven to zero, otherwise it shall be placed in a high impedance state. The Link completes the reset by reasserting LPS after waiting for $T_{LPS\_RESET\_WAIT}$ and then following the initialization procedure as specified in 5.1.1. below.

The Link requests the PHY to suspend the interface by deasserting LPS for a minimum of $T_{LPS\_SUSPEND\_WAIT}$. The interface is re-enabled by the Link reasserting LPS at any time after it sees the PHY withdraw SClk, and then following the initialization procedure as specified in 5.1.1 below.

Note: typically the Link will re-enable the interface in response to a LinkOn signal from the PHY.

If the PHY observes LPS logically deasserted for T_{LPS_RESET} (as illustrated by figure 5-4), it shall ~~disable and~~ reset the interface. If the PHY observes LPS logically deasserted for $T_{LPS\_SUSPEND\_WAIT}$ (as illustrated by figure 5-nn) it shall suspend the interface. The voltage levels show in figures 5-4 and 5-nn for Ctl[0:1], D[0:n], LReq and SClk while LPS is logically deasserted are accurate only for a undifferentiated interface, but the timing relationships remain accurate for both modes.

When the interface is undifferentiated, the PHY resets the interface by driving Ctl[0:1] and D[0:n] ~~and SClk~~ to zero. Otherwise, the PHY resets the interface by placing the Ctl[0:1] and D[0:n] ~~and SClk~~ signals in a high-impedance state.

When the interface is undifferentiated, the PHY suspends the (already reset) interface by driving SClk to zero. Otherwise, the PHY suspends the interface by placing the SClk signal in a high-impedance state.

Modify Figure 5-4 to show SClk present during PHY/Link interface reset, and to show min./max timings (T_{LPS_WAIT} starting from when LPS is deasserted).

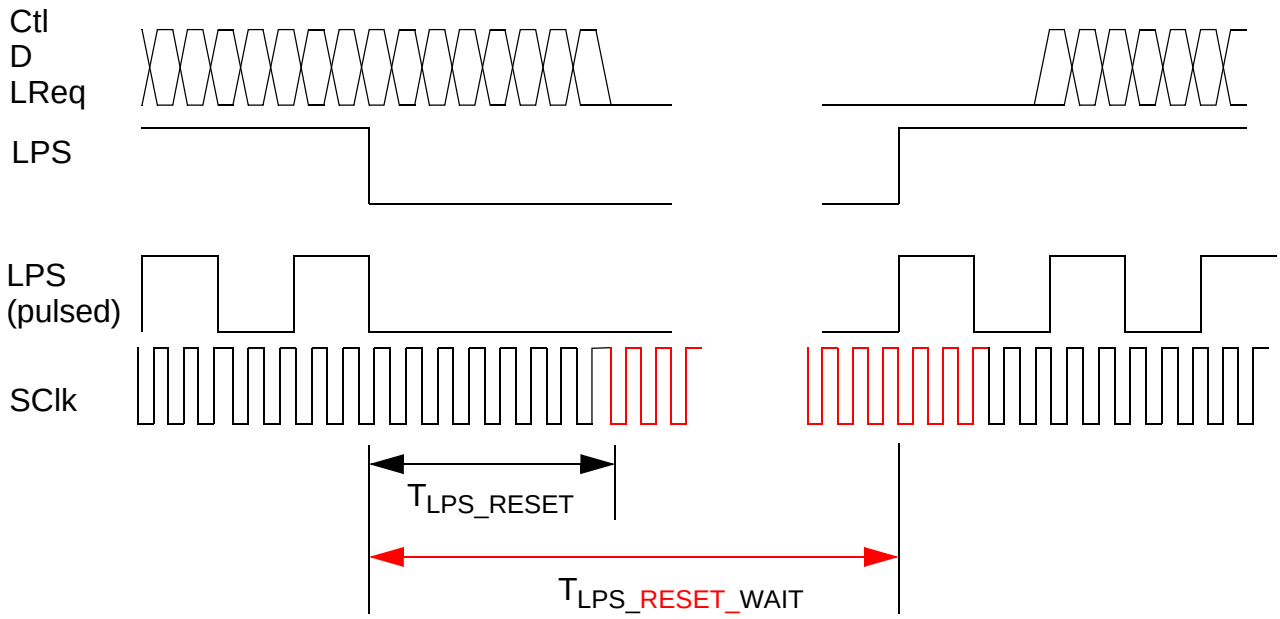

Figure 5-3 - PHY-Link reset timing

Add a new figure to show PHY-Link suspend timing

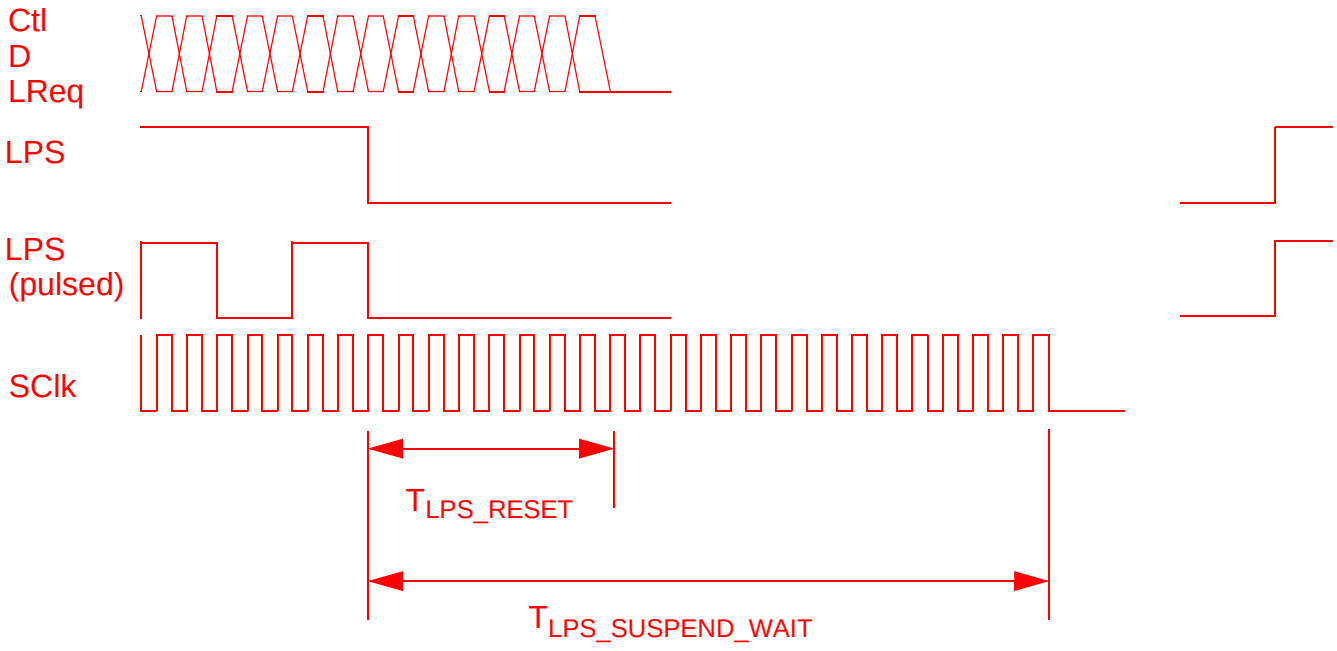

Figure 5-nn - PHY-Link suspend timing

Modify the paragraphs describing resumption as follows:-

The handshake just described resets the interface when the link deasserts LPS for a minimum of 2.75 µs, and suspends it when the Link deasserts LPS for a minimum of 25.5 µs. Normal operation may be restored if the link reasserts LPS (as described in 5.1.1 below).

5.1.1 Interface Initialization

During power-on reset, all outputs are undefined until the operating mode (differentiated or undifferentiated) can be determined. If operating in undifferentiated mode, then some or all outputs may be taken to zero, otherwise all outputs shall be held in high impedance.

Implementation means of setting configurable bits shall be sensed at the moment that power-on-reset completes. If operating in undifferentiated mode all outputs shall then be taken to zero.

Following a power reset or a PHY link interface reset, the link continues the initialization of the interface by asserting LPS. After observing LPS, the PHY shall resume SClk (if necessary) within 2 SClk periods if it is asserting LinkOn, otherwise it shall resume SClk as soon as possible. If the interface is in differentiated mode, the PHY shall resume SClk by driving it low for half a SClk period.

Once SClk is provided ~~resumes~~ the PHY and link shall condition their Ctl[0:1] and D[0:n] outputs in accordance with table 5-3. In this table, the link counts SClk cycles from the later of (i) the time it detects SClk and (ii) the time it provides LPS, and the PHY counts SClk cycles from the later of (i) the time it provides SClk and (ii) the time it detects the presence of LPS.

Delete the phrase “the resumed” in Table 5-3 (four places)

Editorial - I suggest starting clause 5.1 with the description of the initialization of this interface (suggested as Clause 5.1.1 above), and then describe reset and suspend.

3. Further discussion

It should be observed that, as the link/application layer is dependent on the PHY’s clock, the class of devices able to benefit from this change does not include devices in which the link/application is required to run whilst the PHY core is suspended, or the PHY is otherwise not powered. Such devices will require a separate clock to be provided to the link/application.

However, the original proposal was also limited to applications where the only method of bringing the PHY out of suspend was an event on the serial bus. This revised proposal removes this limitation - an external application-related event may now result in the assertion of LPS, which will bring the PHY out of suspend and then the Link out of suspend (subject to final details of the Suspend/Resume proposal).

This proposed specification for initialization of the interface operates in various possible scenarios as follows:-

1) Power on reset, link provides an immediate continuous LPS signal

The PHY will not generate a LinkOn. It provides SClk as soon as POR is completed. The PHY and the Link count the interface reset cycles by reference to the first edge of SClk sent by the PHY.

2) Power on reset, link does not provide LPS

The PHY will wait until the Link (or the Link power management logic) will at some time later provide LPS. On detecting the rising edge of LPS, the PHY will provide SClk within two cycles. The PHY and the Link count the interface reset cycles by reference to the first edge of SClk sent by the PHY.

3) Resumption from Suspend initiated by the Link (Link provides LPS)

The PHY gets its clocks going if necessary, and then provides SClk. The PHY and the Link count the interface reset cycles by reference to the first edge of SClk sent by the PHY

4) Resumption from Suspend initiated by the PHY (Link is not providing LPS)

The PHY will wait until its internal clocks are nice and stable, and then will provide a LinkOn (following the suspend/resume rules). The Link (or the Link power management logic) will at some time later provide LPS. On detecting the rising edge of LPS, the PHY will provide SClk within two cycles. The PHY and the Link count the interface reset cycles by reference to the first edge of SClk sent by the PHY.

5) PHY Link reset

The Link reasserts LPS between 3 and 12.5 us after deasserting it. SClk runs continuously. The PHY and the link count the interface reset cycles by reference to the first SClk cycle sent by the PHY after the link asserts LPS. Note that the Link may count from one SClk cycle earlier than the PHY. This has no effect on correct functioning of the interface, as the current cycle counting rules already provide sufficient guardband.