Cable HOP Considerations

97-089R1

This section describes the design criteria to be used in determining a practical number of cable hops for a 1394 interconnect model prior to the point where the power being delivered by a power provider to the cable bus no longer meets minimum requirements for a newly connected node.

The following list of criteria establish the basis from which the recommendations are made.

Power pair dc resistance
The dc resistance of the power wires (4.5 meters) shall be:

$R_{PV} \leq 0.333\ \Omega$
$R_{PG} \leq 0.333\ \Omega$

Where R_{PV} is the DC resistance of the V_p wire and R_{PG} is the DC resistance of the V_g wire in the power pair in the 1394 cable. Connector to receptacle contact resistance shall not be greater than 0.030 Ω (0.60 Ω per cable)

This resistance number includes the interconnect resistance of the mated pairs (connector and receptacle) at both ends of the cable.

In addition, V_g shall be connected to the inner cable shield at both ends of the cable (reference IEEE 1394-1995 clause 4.2.1.3, figure 4-9 - reducing the effective resistance of V_g to $\cong 0.167\ \Omega$.

The power wires (V_g and V_p) may be constructed using 22 AWG (7x30). Power wire DC resistance shall not exceed 0.273 Ω for a length of 4.5 meters.

Output current per port
The maximum allowed current that may pass through any single port shall be 1.5 Amperes.

Voltage drop through the cable
Two power wire voltage drops need consideration: 1) V_{pir} (determines voltage level available at the V_p pin of a target power consumer), 2) V_{gdif} (determines the ground difference potential between nodes).

The maximum V_p wire voltage drop measured across the cable from the source receptacle to the destination receptacle (including mated connector resistance at both ends), shall be 0.5 V (1.5 A x 0.333 Ω). This implies a maximum cable length of 4.5 meters long with 22 AWG wire. Longer cables may be implemented if the maximum resistance through the cable is maintained. For example, a 12 meter cable, if constructed correctly, could meet the maximum resistance with 18 AWG (19/30) wire.

Ground difference potential may be of concern for safety reasons. Ground difference potential is measured across the V_g wire from the source receptacle to the destination receptacle (including mated connector resistance at both ends). Ground potential difference shall not exceed 0.5 volts.

Device minimum input requirements
A device may consume up to 3 watts of power upon power-up and requires a minimum of 8.0 Volts at its V_p pin on the circuit board side of the connector.

Port-to-Port IR drop
In certain configurations the port-to-port IR drop can be as high as the resistance sum of the interconnecting copper printed circuit board trace and two current limit devices multiplied by the maximum throughput current.

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The maximum port-to-port resistance shall be 0.5 Ω.

Maximum port-to-port resistance includes 0.04 Ω copper PCB trace resistance and 0.46 Ω current limit device resistance (0.23 Ω per current device).

Discussion

Given the absolute numbers above, several models can be examined from very basic home or office models to "LAN"-type set-ups. Figures 0-1 and 0-2 present two models (perceived to be typical for their respective environments) with which the 1394 cable can be connected.

Multiple iterations of either or both of the typical "models" may be connected together to form simple or complex interconnects.

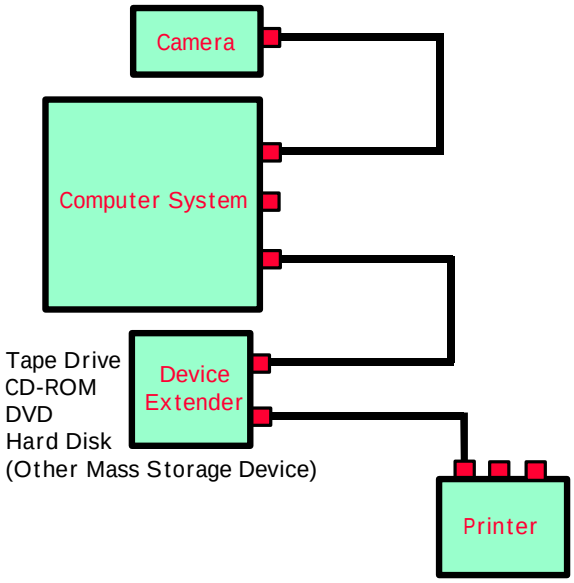

Figure 0-1 -- Typical "PC" 1394 Device & Interconnect

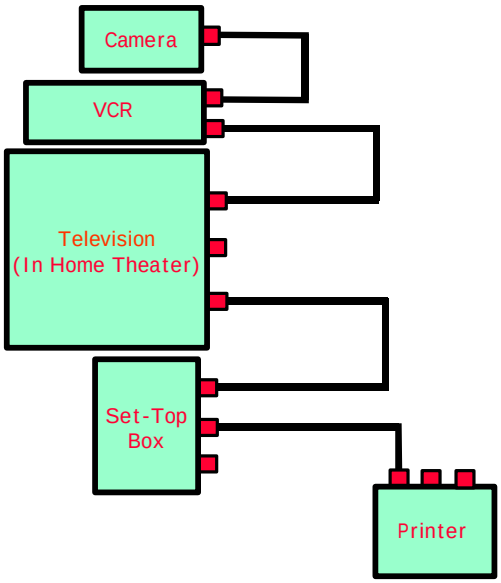

Figure 0-2 -- Typical "CE" 1394 Device & Interconnect

Analysis performed assumes a single power provider delivering power to a leaf node (power consumer) through a series of daisy-chained interconnects (i.e. the devices between the Power Provider and the Power Consumer are power pass-through nodes).

Through the use of constants and assumptions previously provided, useful guidelines can be developed to determine the largest number of cable hops that can be supported for a variety of power provider implementations. The determination for what the maximum number of cable hops that can be supported, given a specific power provider capacity, is based upon the voltage and power available at the V_p input pin on the circuit board side of the target Power Consumer connector.

The minimum voltage required for node enumeration is 7.5 volts. The column labeled "Max. Hops (V_{min})" identifies the maximum number of cable hops before available input voltage drops below 7.5 volts.

The minimum power required for node enumeration may be as high as 3 Watts (a PHY may consume up to three watts on power-on reset). The column labeled "Max. Hops (W_{min})" identifies the maximum number of cable hops before available input power drops below 3 Watts.

In choosing the maximum cable hops for a particular power provider capacity, choose the lower number of hops between HOPS (V_{min}) and HOPS (W_{min}).

POWR_CLASS	Current Drawn Through Cable	Output Launch Voltage	Max. Hops (W_{min})	Max. Hops (V_{min})
001_2	0.750	20	25	19
	0.625	24	36	31
	0.577	26	42	38
	0.500	30	57	53
	0.455	33	69	66
010_2	1.500	20	14	9
	1.250	24	20	15
	1.150	26	24	18
	1.00	30	32	26
	0.909	33	38	33
011_2	1.50	30	22	17
	1.36	33	26	22

The values in the table above were determined by using:

Power = Current^2 * Resistance Voltage = Current * Resistance

where:

Current = Bus Current Maximum Values (0.75 amps, 1.0 amps, 1.25 amps, 1.5 amps)
Voltage = Power Provider Launch Voltage (20 volts, 24 volts, 30 volts)
Resistance = V_p Power Wire Resistance + Port-to-Port Resistance
V_p Power Wire Resistance = 0.333 Ω (Cable length equals 4.5 meters[1])
P-to-P Resistance = 0.500 Ω

[1]Note: Cable lengths longer than 4.5 meters may be constructed, however, they must still meet the maximum V_p power wire resistance of 0.333 Ω. This may be achieved by using a larger AWG wire to construct the cable.

Kirchoff's voltage law is used to determine the voltage available at the Vp pin of each node as represented by the following analysis example of a two hop interconnect:

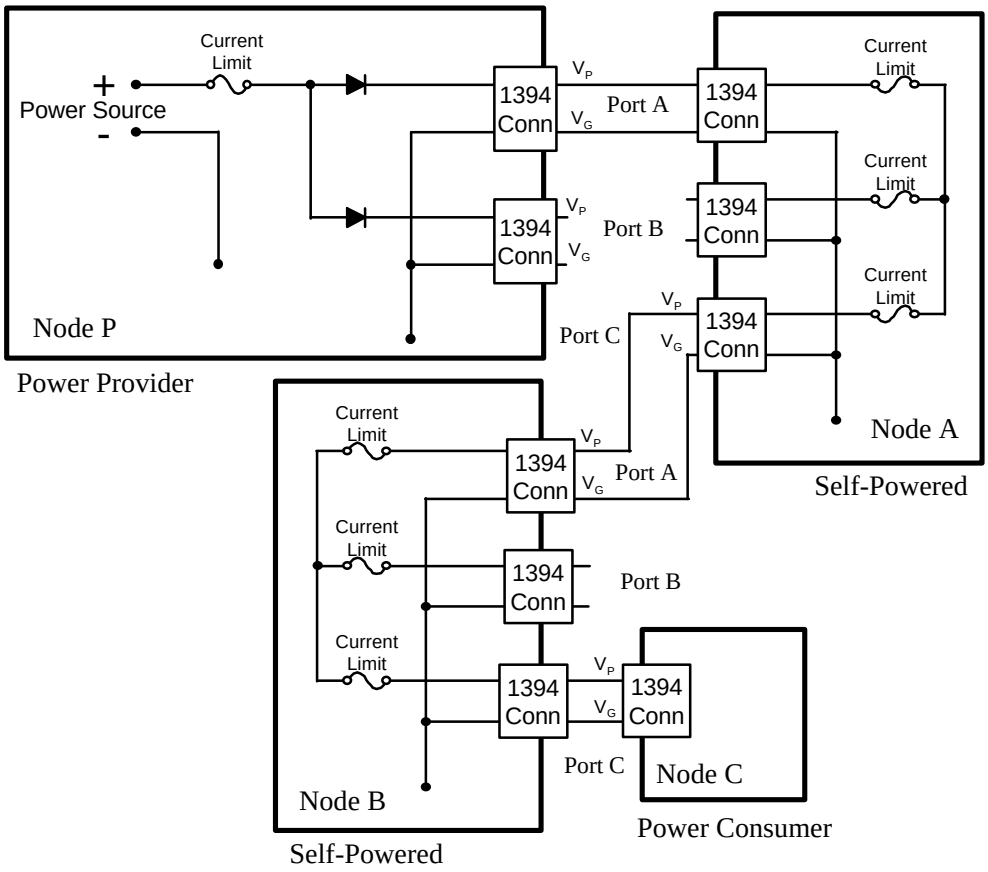

Figure 0-3 - Two-Hop Interconnect Example

In this example, the following analysis applies:

Assume the power provider capacity is 30 Watts at a launch voltage of 26 Volts (as measured at the V_p pin on the receptacle side of Node P, Port A). Further, assume the Power Consumer (Node C) draws 1.15 amperes. All cable interconnects are 4.5 meters in length.

Using the constants previously defined, the voltage drop across the V_p power wire in the cable connecting Node P, Port A and Node A, Port A is equal to the current drawn through the wire multiplied by the resistance of the wire and connector/receptacle resistance (E = IR). The current is 1.15 amperes. The maximum wire resistance is equal to 0.273 ohms. The connector contact resistance (0.60 ohms) for a total wire interconnect DC resistance of 0.333 Ohms. The voltage drop across this connection is equal to 0.383 volts (NWC_1).

The current now must flow through the circuit board interconnect copper trace and two current limit devices before being presented out Port C of Node A. The voltage drop here is equal to 1.15 X 0.5 Ohms = 0.575 Volts (PPC_1).

The voltage drop across the power wire connecting Port C of Node A to Port A of Node B is calculated exactly like the IR drop for NWC_1 and is also equal to 0.383 Volts (NWC_2).

The voltage drop through the Node B Port A and Port C is calculated the same as the IR drop for PPC_1 and is also equal to 0.575 Volts (PPC_2).

The voltage drop across the power wire connecting Port C of Node B to the port on Node C is calculated exactly like the IR drop for NWC_1 and NWC_2 and is also equal to 0.383 volts (NWC_3).

The voltage available at the V_p pin on the circuit board side of the port on Node C is equal to the voltage supplied by the power provider less the sum of the voltage drops across the interconnects to Node C. Thus:

V_p at port Node C = V_p at Port A Node P - NWC_1 - PPC_1 - NWC_2 - PPC_2 - NWC_3.

V_p at port Node C = 26 Volts - 0.383 Volts - 0.575 Volts - 0.383 Volts - 0.575 Volts - 0.383 Volts.

V_p at port Node C = 26 Volts - 2.299 Volts

V_p at port Node C = 23.7 Volts

Similarly, the power capacity available at the Vp pin of the port on Node C can be calculated using the power formula $P = I^2R$. The power drop should be calculated for each leg for which the voltage drop was calculated. The power available is equal to the power capacity of the power provider less the sum of the individual interconnect power drops.

The power capacity at the V_p pin of the port at Node C is equal to 27.4 Watts.