Provision of SClk on Power-On reset

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At the informal PHYDOGs meeting today we identified an issue which we agreed needed wider review before "consensus" could be deemed.

Various current PHY devices behave in different ways with respect to the provision of SClk at power on. We believe that it is useful to specify this behaviour in the standard. In addition, we have agreed a detailed specification for start-up of the PHY link interface once LPS has been asserted as part of an interface reset protocol (see P1394a/97-079r2), and we believe that this should be leveraged at POR time. It is also useful to define the behaviour of all the lines on the PHY/link interface at POR time.

We therefore make the following proposal for discussion now and decision in Houston (possibly in modified form following reflector discussion).

Effect at Power-On-Reset

During POR

- all outputs are undefined until the operating mode (differentiated or undifferentiated) can be determined. If operating in undifferentiated mode, then all outputs are taken to zero, otherwise all outputs are held in high impedance.

At the end of POR

- implementation means of setting configurable bits are sensed at the moment that POR completes
- PHY/Link start-up is as per start-up in the PHY/Link reset spec (SClk is provided in response to LPS)
- (Then normal specifications apply)

Rationale:-

The PHY should not send a dirty SClk (which could happen if SClk is provided before the PHY's internal clocks have settled)
The PHY must not send SClk until it can process LPS (and then only if LPS allows) - unsolicited SClk is not allowed
The PHY cannot complete the PHY/link reset process until after the end of POR (it can't count cycles or assert the special handshake Data_prefix
If a clock is required during Link POR, then it is possible to set the timer on Link POR to be sufficiently longer than PHY POR and assert LPS during Link POR