1. Combined Timing Constants

Table 1 represents the combination of PHY constants from P1394a 1.2 and 1394-1995. The shaded rows indicate which constants are only defined in 1394-1995 and which must be referenced for P1394a PHY design.

Table 1: Cable PHY timing Constants

Timing Constant	Minimum	Maximum	Comment
ACK_RESPONSE_TIME	40 ns	240 ns	Idle time measured at the cable connector from the end of DATA_END that follows a primary packet to the start of DATA_PREFIX that precedes the acknowledge packet.
ARB_RESPONSE_DELAY	33.3 ns	PHY_DELAY	Delay between an RX_REQUEST signal arriving at the receiving port and the TX_REQUEST signal being sent at the transmit port(s).
ARB_SPEED_SIGNAL_START	-0.02 µs		Time delay between a transmitting port generating the data_prefix signal and the same transmitting port generating the transmission speed signal
BUS_TO_LINK_DELAY	PHY_DELAY		Data propagation time measured from the Serial Bus connector to the PHY/link interface.
BASE_RATE	98.294 Mbit/s	98.314 Mbit/s	Base bit rate (98.304 ± 100 ppm) Mbit/s
CONCATENATION_PREFIX_TIME	160 ns		At a transmitting port, the time between the end of clocked data and the start of speed signaling (when present) for the concatenated packet that follows.
CONFIG_TIMEOUT	166.6 µs	166.9 µs	Loop detect time (~16384/BASE_RATE)
CONNECT_TIMEOUT	336.0 ms	341.3 ms	Connection debounce time
DATA_END_TIME	0.24 µs	0.26 µs	End of packet signal time (~24/BASE_RATE)
DATA_PREFIX_HOLD	40 ns		At a transmitting port, the time between the end of speed signalling (when present) and the start of clocked data.
DATA_PREFIX_TIME			This timing constant is no longer defined; see DATA_PREFIX_HOLD and MIN_DATA_PREFIX.
FORCE_ROOT_TIMEOUT	83.3 µs	CONFIG_TIMEOUT	Time to wait in state T0 (Tree-ID Start; see 4.4.2.2) before acknowledging Parent_notify signals. (between ~8192/BASE_RATE and ~16384/BASE_RATE) **Important**: This time shall be less than or equal to the CONFIG_TIMEOUT value for the node.
LINK_TO_BUS_DELAY	40 ns	100 ns	Data propagation time measured from the PHY/link interface to the Serial Bus connector.
MAX_ARB_STATE_TIME	200 µs	400 µs	Maximum time in any state (before a bus reset shall be initiated) except the idle state or a state that exits after an explicit time-out.
MAX_BUS_HOLD		1.63 µs	Maximum time a node may transmit a TX_DATA_PREFIX signal between the request acknowledge and data packet of concatenated asynchronous subactions or between data packets of concatenated Isochronous subactions. The link shall ensure that this time is not exceeded.
MAX_BUS_OCCUPANCY			This timing constant is no longer defined; see MAX_DATA_TIME.
MAX_DATA_TIME		84.31 µs	The maximum time that clocked data may be transmitted continuously. If this limit is exceeded, unpredictable behavior may result.
MAX_DATA_PREFIX_DELAY		PHY_DELAY (see table 4-29)	Maximum delay between a RX_DATA_PREFIX signal arriving at a receive port and a TX_DATA_PREFIX being sent at a transmit

			port (this means that the data prefix signal has to be delayed less than the clocked data)
MIN_DATA_PREFIX	140 ns		The total time an originating port transmits a TX_DATA_PREFIX signal prior to clocked data.
MIN_PACKET_SEPARATION	0.34 µs		Minimum time between packets (~32/BASE_RATE)
NOMINAL_CYCLE_TIME	124.988 µs	125.013 µs	Average time between the start of one isochronous cycle and the next (125 µs ± 100 ppm)
PHY_DELAY	80 ns	See PHY registers	Best-case repeater data delay has a fixed minimum.
PING_RESPONSE_TIME	50 ns	240 ns	Time permitted a PHY to respond to a ping packet (see clause 7.4.5), measured at the connector from the end of DATA_END to the start of DATA_PREFIX for the first self-ID packet.
RESET_DETECT	80.0 ms	85.3 ms	Time for a connected node to confirm a reset signal
RESET_TIME	166.6 µs	166.7 µs	Reset hold time (~16384/BASE_RATE)
RESET_WAIT	0.16 µs		Reset wait delta time. (~16/BASE_RATE)
ROOT_CONTEND_FAST	0.76 µs	0.80 µs	Time to wait in state T3: Root Contention if the random bit is zero, as described in clause 4.4.2.2 of IEEE Std 1394-1995. (~80/BASE_RATE)
ROOT_CONTEND_SLOW	1.60 µs	1.64 µs	Time to wait in state T3: Root Contention if the random bit is one, as described in clause 4.4.2.2 of IEEE Std 1394-1995. (~160/BASE_RATE)
SHORT_RESET_TIME	1.30 µs	1.40 µs	Short reset hold time. (~128/BASE_RATE)
SID_SPEED_SIGNAL_START	-0.02 µs	0.02µs	Time delay between a child port generating the TX_IDENT_DONE signal and the same child port generating the speed capability signal
SPEED_SIGNAL_LENGTH	0.10 µs	0.12 µs	Time while speed signaling is active (~10/BASE_RATE)

2. Suggested Changes

Based on our consensus review at the PHYDOG's meeting in Albuquerque, the following modifications are proposed for P1394a to clarify intent, correct errors, etc.

Table Title

Some of the parameters in the table are not guaranteed by the PHY, but are required to characterize a node's behavior at the 1394 interface. One example is NOMINAL_CYCLE_TIME. Proposal is to change the table title to "Cable interface timing constants" since the constants are node specific rather than PHY specific.

ACK_RESPONSE_TIME → MAX_RESPONSE_TIME

Per the Albuquerque PHY designer's review session, this parameter is intended to subsume the PING_RESPONSE_TIME and specifies the time by which a node must commence any response required to be received before a subaction_gap is detected anywhere within the network. Responses which must be received within the same subaction include acknowledge packets, isochronous packets, remote reply packets, self-id packets, and TX_SUSPEND/TX_DISABLE indications. Consequently, the comment should be updated to:

> Idle time measured at the cable connector from the end of DATA_END that follows a primary packet, ping packet, remote access packet or remote reply packet to the start of the DATA_PREFIX for an ACK packet, a self_ID packet, a remote reply packet, an isochronous packet, or a TX_SUSPEND or TX_DISABLE. See Figure 4.

ARB_RESPONSE_DELAY

This timing parameter was intended to bound the PHY's response to any received arbitration indication. It defines the time for repeating a TX_REQUEST signal, the delay of DATA_PREFIX through the node, etc. It subsumes the MAX_DATA_PREFIX_DELAY parameter as well. The comment needs to be updated:

> Arbitration delay of a node measured between the start of reception of an arbitration signal at the receiving port and the start of transmission of a corresponding arbitration indication at any port (including the initial receive port).
>
> Note: The maximum specification of PHY_DELAY guarantees that arbitration indications are repeated no slower than clocked data.

ARB_SPEED_SIGNAL_START

This parameter only applies to the first packet after IDLE or RX_GRANT. Said differently, this parameter does not specify the relationship of the speed signaling to the DATA_PREFIX of concatenated packets. As such, the comment should be clarified and a reference to the figure added:

> Time delay between a transmitting port generating the DATA_PREFIX signal and the same transmitting port generating the transmission speed signal for the first packet in a possible concatenated sequence. See Figure 1.

BUS_TO_LINK_DELAY

This parameter is not required to specify node behavior when viewed from the 1394 interface. In fact, compliance to this parameter can not be determined from the 1394 connector. This parameter was added to aid the "pinging" calculations and the only contribution to the pinging calculation comes from the BUS_TO_LINK_DELAY of the device initiating the ping. In general, the node performing the pinging can know the bus-to-link delay of it's own PHY/LINK combination through non-normative means. Consequently, BUS_TO_LINK should not be part of the normative Clause 7 interface parameters. However, there is a need for nodes that employ discrete PHY's to know the BUS_TO_LINK delay contribution from its attached PHY. As such, BUS_TO_LINK_DELAY should be moved to the timing parameters for Clause 5 and the comment modified to read:

> Delay from receiving DATA_PREFIX on a receive port to transmitting Receive on CTL[0:1] at the PHY/Link interface.

As part of the clause 5 specification, it is also more appropriate to specify timings in terms of SCLK cycles and the MIN/MAX values are recalculated as such.

This change will affect OHCI generic software that may assume BUS_TO_LINK_DELAY applies regardless of whether the PHY is integrated or discrete. The proper fix for this is to add the necessary constants into OHCI, not to constrain integrated PHY designs in P1394a.

CONCATENATION_PREFIX_TIME

When transmitting concatenated packets, originating and repeating PHY's shall ensure that CONCATENATION_PREFIX_TIME + SPEED_SIGNAL_LENGTH + DATA_PREFIX_HOLD is met even when no speed-signaling is present. The comment for CONCATENATION_PREFIX_TIME should be adjusted to suggest that the speed signaling time is always required and to reference the appropriate figure:

> At a transmitting port, the time between the end of clocked data and the start of the speed signaling time for the concatenated packet that follows. See Figure 3.

DATA_END_TIME

A figure illustrating the end of packet transmission has been prepared and should be referenced in the comment:

> End of packet signal time (~24/BASE_RATE). See Figure 3.

DATA_PREFIX_HOLD

When transmitting concatenated packets, originating and repeating PHY's shall ensure that CONCATENATION_PREFIX_TIME + SPEED_SIGNAL_LENGTH + DATA_PREFIX_HOLD is met even when no speed-signaling is present. The comment for DATA_PREFIX_HOLD should be adjusted to suggest that the speed signaling time is always required and to reference the appropriate figures:

> At a transmitting port, the time between the end of the speed signaling time and the start of clocked data. See Figure 1 and Figure 2.

LINK_TO_BUS _DELAY

This parameter is not required to specify node behavior when viewed from the 1394 interface. In fact, compliance to this parameter can not be determined from the 1394 connector. This parameter was added to aid the "pinging" calculations and the only contribution to the pinging calculation comes from the LINK_TO_BUS_DELAY of the device initiating the ping. In general, the node performing the pinging can know the link-to-bus delay of it's own PHY/LINK combination through non-normative means. Consequently, LINK_TO_BUS should not be part of the normative Clause 7 interface parameters. However, there is a need for nodes that employ discrete PHY's to know the LINK_TO_BUS delay contribution from its attached PHY. As such, LINK_TO_BUS_DELAY should be moved to the timing parameters for Clause 5 and the comment modified to read:

> Delay from first Idle on CTL[0:1] in which the link releases the PHY/Link interface to the start of DATA_END following the originated packet on all transmit ports.

As part of the clause 5 specification, it is also more appropriate to specify timings in terms of SCLK cycles and the MIN/MAX values are recalculated as such.

This change will affect OHCI generic software that may assume LINK_TO_BUS_DELAY applies regardless of whether the PHY is integrated or discrete. The proper fix for this is to add the necessary constants into OHCI, not to constrain integrated PHY designs in P1394a.

MAX_BUS_HOLD

With fly-by acceleration, asynchronous concatenations can occur on the ack following both request and response primary packets. Consequently, MAX_BUS_HOLD should be extended to the total amount of DATA_PREFIX between the acknowledge of any primary asynch packet and the following concatenated primary packet. Furthermore, only the node originating the concatenation can be responsible for enforcing MAX_BUS_HOLD. As such, the MAX_BUS_HOLD comment should be modified to read:

> Maximum time an originating node may transmit a TX_DATA_PREFIX signal between concatenated packets. The link shall ensure that this time is not exceeded.

When a discrete PHY is employed, the attached link is responsible for ensuring MAX_BUS_HOLD is met. However, the current P1394a draft doesn't provide sufficient information for the link to guarantee it doesn't exceed MAS_BUS_HOLD. For example, the link doesn't know how long the PHY asserts DATA_PREFIX on the wire before granting the link. To ensure a discrete PHY and link cooperate to properly meet MAX_BUS_HOLD, two new parameters are defined for inclusion in Clause 5. (The parameters are not externally visible and only pertain to the PHY/Link interface.)

MAX_DATA_PREFIX_TO_GRANT bounds the duration of the DATA_PREFIX the PHY asserts on the 1394 bus before granting the link to transmit. The precise definition is given as:

> Delay from PHY first sending DATA_PREFIX at a port to asserting Grant on CTL[0:1] at the PHY/Link interface.

MAX_HOLD_CYCLES limits the number of HOLD indications the link can use to delay transmission of a packet once the interface has been granted by the PHY. The precise definition is given as:

> Maximum duration of consecutive HOLD indications the link can drive on CTL[0:1] after sampling Grant and before asserting Transmit.

Since the PHY/Link interface can take as many as three cycles to turn around (GRANT-IDLE-IDLE), the DATA_PREFIX time on the 1394 bus between concatenations can be given (in cycles) as MAX_DATA_PREFIX_TO_GRANT + 3 + MAX_HOLD_CYCLES + LINK_TO_BUS_DELAY. With the proposed parameters, the maximum DATA_PREFIX time caused by the link during concatenation will be 80 cycles or 1627 ns, just shy of the 1630 ns MAX_BUS_HOLD requirement.

MAX_DATA_PREFIX_DELAY

This parameter is superceded by ARB_RESPONSE_DELAY which, for the purpose of gap count analysis, bounds the minimum and maximum time the PHY uses to repeat or respond to any received arbitration indication (not just DATA_PREFIX). Comment becomes:

> This timing constant is no longer defined; see ARB_RESPONSE_DELAY.

MIN_DATA_PREFIX

This parameter only applies to the first packet after IDLE or RX_GRANT. Said differently, this parameter does not specify the duration of DATA_PREFIX in between concatenated packets. As such, the comment should be clarified and a reference to the figure added:

> The total time an originating port transmits a TX_DATA_PREFIX signal prior to clocked data. This constant is not applicable to data prefix that precedes a concatenated packet (see CONCATENATION_PREFIX_TIME). See Figure 1.

MIN_IDLE_TIME

All nodes must enforce a minimum idle gap after the DATA_END of a packet sequence. This minimum time used to be accounted for by the minimum ACK_RESPONSE_TIME. However, ACK_RESPONSE_TIME and the new MAX_RESPONSE_TIME only apply at the originating node. Consequently, a new parameter that applied at every transmitting port was required. The definition of MIN_IDLE_TIME is:

> Idle gap separating packets at any port of an originating or repeating node. See Figure 3.

MIN_PACKET_SEPARATION

This parameter only applies to the duration of DATA_PREFIX between concatenated packets and is only enforced at the node that originates the concatenation. Also, the originally specified guideline of ~32/BASE_RATE is in error. The .34 µS minimum is actually closer to ~34/BASE_RATE. The comment should also include a reference to the new figure:

> The total duration of the TX_DATA_PREFIX signal separating clocked data of concatenated packets at any port of an originating node. See Figure 2.
> (~34/BASE_RATE)

PHY_DELAY

To allow for the possibility of faster PHY's, the minimum delay should be reduced to 60 ns. The minimum parameter was originally included to aid in the gap count optimization. Consequently, the 20 ns reduction is not significant.

PING_RESPONSE_TIME

This parameter is superceded by the MAX_RESPONSE_TIME constant which defines the max Idle time that can be sustained at any originating port while still ensuring a subaction_gap isn't detected in the network. Such a parameter is needed for more than just acks and pings. Comment becomes:

> This timing constant is no longer defined; see `MAX_RESPONSE_TIME`.

SPEED_SIGNAL_LENGTH

The speed signaling period must be guaranteed by any transmitting port. This is true even in the case of S100 when no speed code is actually signaled. The comment should clarify this requirement and reference the new diagrams:

> Duration of speed signaling at a transmitting port. See Figure 1 and Figure 2.
> (~10/BASE_RATE)
>
> **Important:** This time period is required for S100 packet transmission even though an explicit speed signal is not sent.

3. Updated Tables

Table 2 provides a single table of all Clause 7 constants complete with all of the proposed modifications. The intent is to have Table 2 complete replace Table 4-32 from the IEEE1394-1995 specification. This will allow designers to clearly see all of the necessary constants in a single consistent location.

Table 3 contains the interface constants which should be moved into Clause 5 since they pertain only to the PHY/Link interface.

Table 2: Cable interface timing constants

Timing Constant	Minimum	Maximum	Comment
ARB_RESPONSE_DELAY	33.3 ns	PHY_DELAY	Arbitration delay of a node measured between the start of reception of an arbitration signal at the receiving port and the start of transmission of a corresponding arbitration indication at any port (including the initial receive port). Note: The maximum specification of PHY_DELAY guarantees that arbitration indications are repeated no slower than clocked data.
ARB_SPEED_SIGNAL_START	-0.02 µs		Time delay between a transmitting port generating the DATA_PREFIX signal and the same transmitting port generating the transmission speed signal for the first packet in a possible concatenated sequence. See Figure 1.
BASE_RATE	98.294 Mbit/s	98.314 Mbit/s	Base bit rate (98.304 ± 100 ppm) Mbit/s
CONCATENATION_PREFIX_TIME	160 ns		At a transmitting port, the time between the end of clocked data and the start of the speed signaling time for the concatenated packet that follows. See Figure 2.
CONFIG_TIMEOUT	166.6 µs	166.9 µs	Loop detect time (~16384/BASE_RATE)
CONNECT_TIMEOUT	336.0 ms	341.3 ms	Connection debounce time
DATA_END_TIME	0.24 µs	0.26 µs	End of packet signal time (~24/BASE_RATE). See Figure 3.
DATA_PREFIX_HOLD	40 ns		At a transmitting port, the time between the end of the speed signaling time and the start of clocked data. See Figure 1 and Figure 2.
DATA_PREFIX_TIME			This timing constant is no longer defined; see DATA_PREFIX_HOLD and MIN_DATA_PREFIX.
FORCE_ROOT_TIMEOUT	83.3 µs	CONFIG_TIMEOUT	Time to wait in state T0 (Tree-ID Start; see 4.4.2.2) before acknowledging Parent_notify signals. (between ~8192/BASE_RATE and ~16384/BASE_RATE) **Important**: This time shall be less than or equal to the CONFIG_TIMEOUT value for the node.
MAX_ARB_STATE_TIME	200 µs	400 µs	Maximum time in any state (before a bus reset shall be initiated) except the idle state or a state that exits after an explicit time-out.
MAX_BUS_HOLD		1.63 µs	Maximum time an originating node may transmit a TX_DATA_PREFIX signal between concatenated packets. The link shall ensure that this time is not exceeded.
MAX_BUS_OCCUPANCY			This timing constant is no longer defined; see MAX_DATA_TIME.
MAX_DATA_TIME		84.31 µs	The maximum time that clocked data may be transmitted continuously. If this limit is exceeded, unpredictable behavior may result.

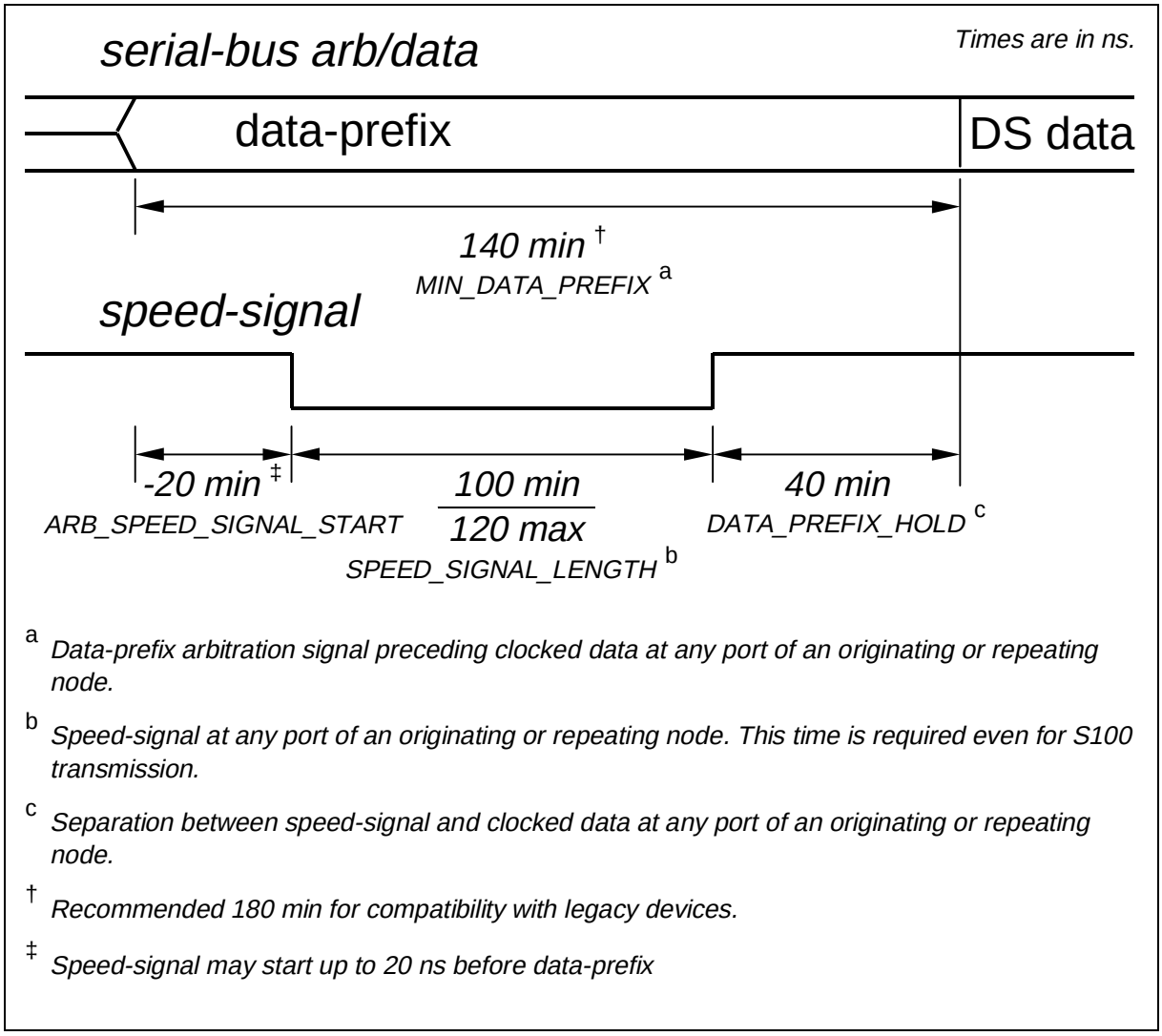
MAX_DATA_PREFIX_DELAY			This timing constant is no longer defined; see ARB_RESPONSE_DELAY.
MAX_RESPONSE_TIME		240 ns	Idle time measured at the cable connector from the end of DATA_END that follows a primary packet, ping packet, remote access packet or remote reply packet to the start of the DATA_PREFIX for an ACK packet, a self_ID packet, a remote reply packet, an isochronous packet, or a TX_SUSPEND or TX_DISABLE. See Figure 4.
MIN_DATA_PREFIX	140 ns		The total time an originating port transmits a TX_DATA_PREFIX signal prior to clocked data. This constant is not applicable to data prefix that precedes a conactenated packet (see CONCATENATION_PREFIX_TIME). See Figure 1.
MIN_IDLE_TIME	40 ns		Idle gap separating packets at any port of an originating or repeating node. See Figure 3.
MIN_PACKET_SEPARATION	0.34 µs		The total duration of the TX_DATA_PREFIX signal separating clocked data of concatenated packets at any port of an originating node. See Figure 2. (~34/BASE_RATE)
NOMINAL_CYCLE_TIME	124.988 µs	125.013 µs	Average time between the start of one isochronous cycle and the next (125 µs ± 100 ppm)
PHY_DELAY	60 ns	See PHY Registers	Best-case repeater data delay has a fixed minimum.
PING_RESPONSE_TIME	50 ns	240 ns	This timing constant is no longer defined; see MAX_RESPONSE_TIME.
RESET_DETECT	80.0 ms	85.3 ms	Time for a connected node to confirm a reset signal
RESET_TIME	166.6 µs	166.7 µs	Reset hold time (~16384/BASE_RATE)
RESET_WAIT	0.16 µs		Reset wait delta time. (~16/BASE_RATE)
ROOT_CONTEND_FAST	0.76 µs	0.80 µs	Time to wait in state T3: Root Contention if the random bit is zero, as described in clause 4.4.2.2 of IEEE Std 1394-1995. (~80/BASE_RATE)
ROOT_CONTEND_SLOW	1.60 µs	1.64 µs	Time to wait in state T3: Root Contention if the random bit is one, as described in clause 4.4.2.2 of IEEE Std 1394-1995. (~160/BASE_RATE)
SHORT_RESET_TIME	1.30 µs	1.40 µs	Short reset hold time. (~128/BASE_RATE)
SID_SPEED_SIGNAL_START	-0.02 µs	0.02µs	Time delay between a child port generating the TX_IDENT_DONE signal and the same child port generating the speed capability signal
SPEED_SIGNAL_LENGTH	0.10 µs	0.12 µs	Duration of speed signaling at a transmitting port. See Figure 1 and Figure 2. (~10/BASE_RATE) **Important:** This time period is required for S100 packet transmission even though an explicit speed signal is not sent.

Table 3: PHY/Link interface timing Constants

Timing Constant	Minimum	Maximum	Comment
BUS_TO_LINK_DELAY	2 cycles	9 cycles	Delay from receiving DATA_PREFIX on a receive port to transmitting Receive on CTL[0:1] at the PHY/Link interface.
LINK_TO_BUS_DELAY	2 cycles	5 cycles	Delay from first Idle on CTL[0:1] in which the link releases the PHY/Link interface to the start of DATA_END following the originated packet on all transmit ports.
MAX_DATA_PREFIX_TO_GRANT		25 cycles	Delay from PHY first sending DATA_PREFIX at a port to asserting Grant on CTL[0:1] at the PHY/Link interface.
MAX_HOLD_CYCLES		47 cycles	Maximum duration of consecutive HOLD indications the link can drive on CTL[0:1] after sampling Grant and before asserting Transmit.

4. Proposed Figures

The following figures were reviewed and adopted at the Albuquerque PHYDOG's meeting.



a *Data-prefix arbitration signal preceding clocked data at any port of an originating or repeating node.*

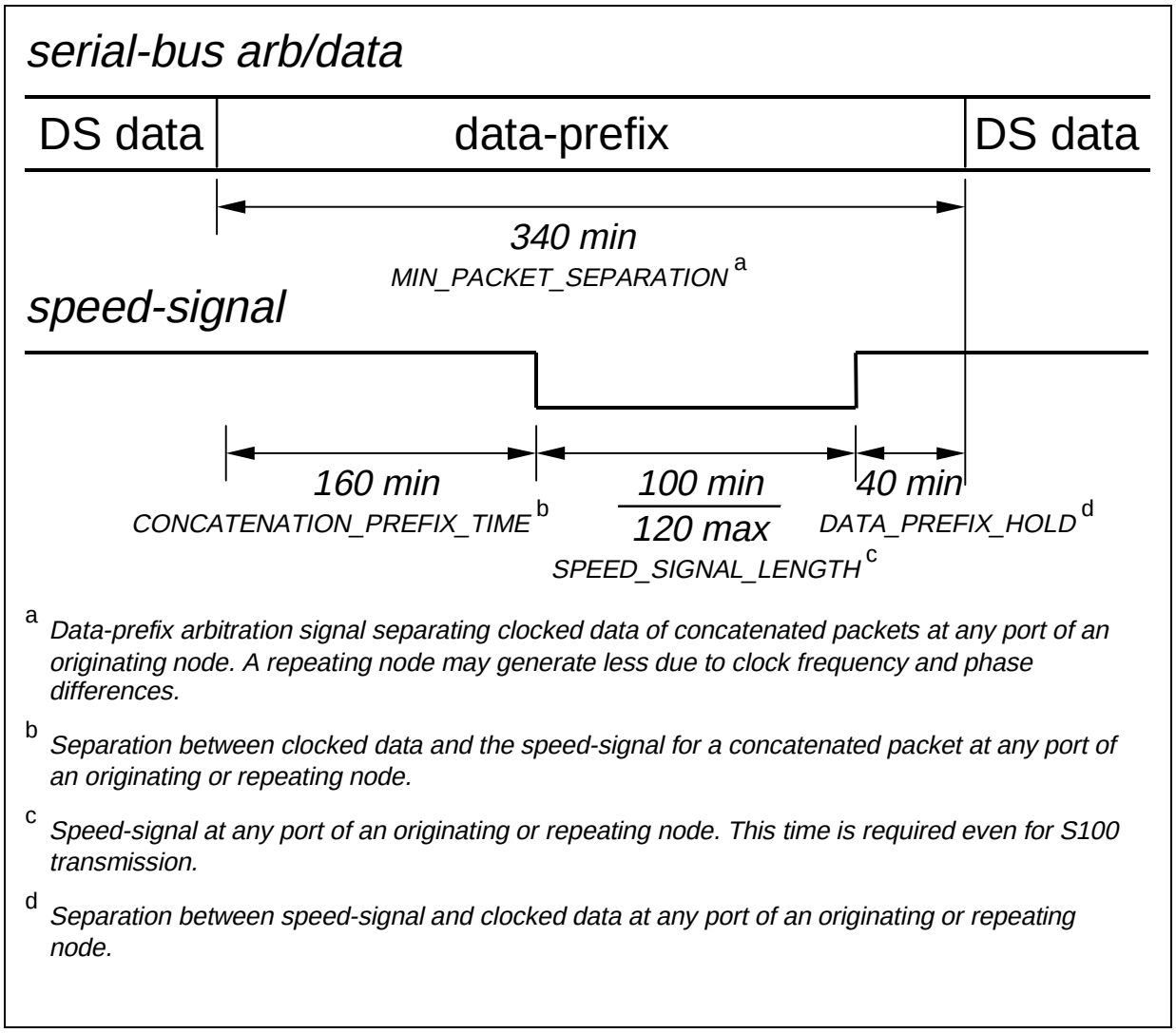
b *Speed-signal at any port of an originating or repeating node. This time is required even for S100 transmission.*

c *Separation between speed-signal and clocked data at any port of an originating or repeating node.*

† *Recommended 180 min for compatibility with legacy devices.*

‡ *Speed-signal may start up to 20 ns before data-prefix*

Figure 1 —Start of packet transmission (first of a possible concatenated sequence)



a *Data-prefix arbitration signal separating clocked data of concatenated packets at any port of an originating node. A repeating node may generate less due to clock frequency and phase differences.*

b *Separation between clocked data and the speed-signal for a concatenated packet at any port of an originating or repeating node.*

c *Speed-signal at any port of an originating or repeating node. This time is required even for S100 transmission.*

d *Separation between speed-signal and clocked data at any port of an originating or repeating node.*

Figure 2 —Concatenated packet transmission

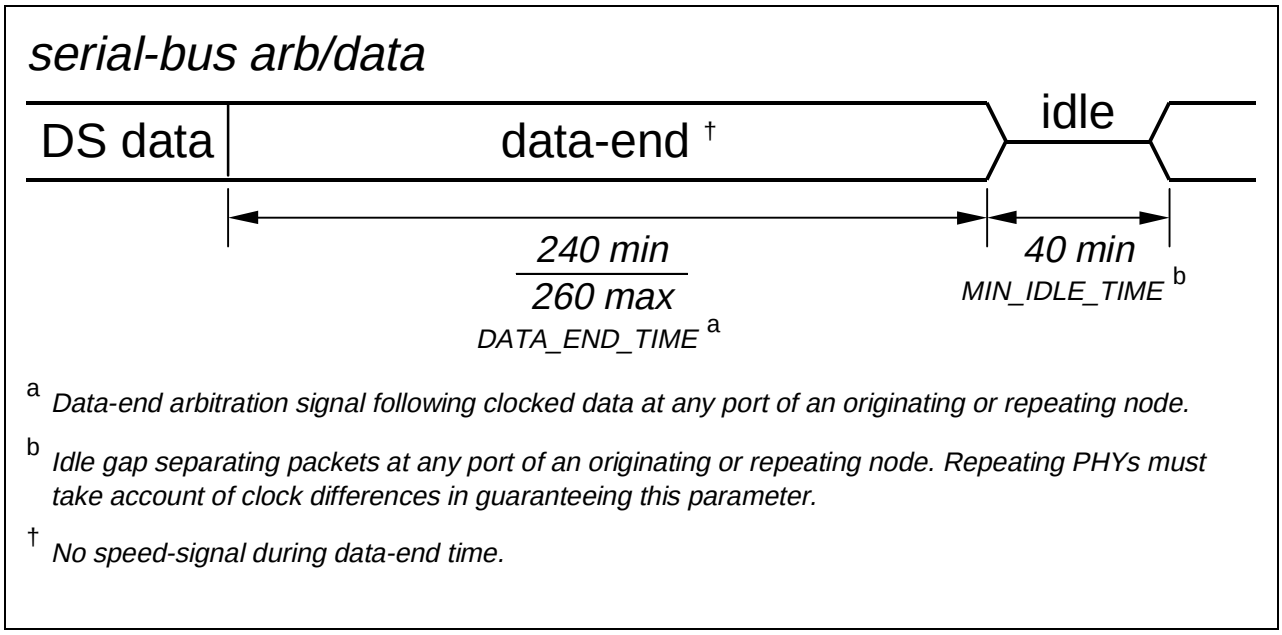


Figure 3 —End of packet transmission

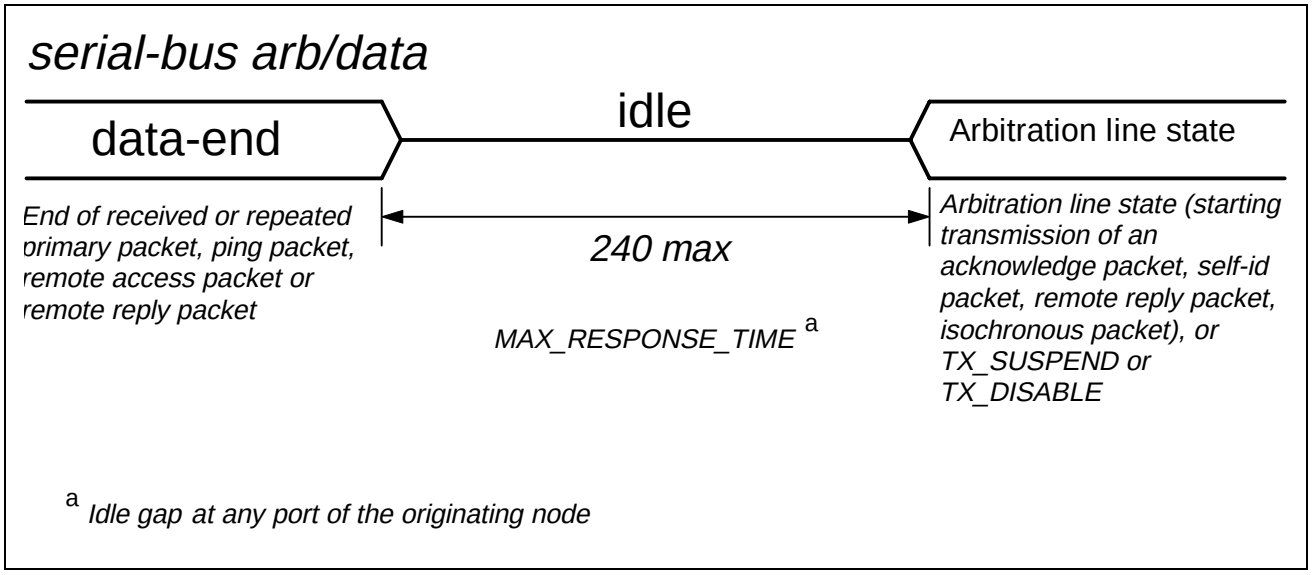


Figure 4 —Response Time to prevent detection of a subaction_gap