After being granted the bus by the Phy, the Link may return control back over to the PHY without transmitting any data. This may be done with or without any "hold" cycles from the link.

Figure 1: Link Cancel using 2-idle cycles as described in section 5.4 of P1394a version 1.3: (note the potential problem cycle where the bus is left floating, it would not be wise for the link to sample the Ctl lines on this cycle!)

PHY Ctl [0:1]	···· 00 11 00 ZZ ZZ ZZ 00 ····
PHY Data [0:n]	00 00 00 ZZ ZZ ZZ 00
	I Bus
Link Ctl [0:1]	···· ZZ ZZ ZZ 00 00 ZZ ZZ ····
Link Data [0:n]	

Figure 2: Link Cancel proposal with 3-idle cycles driven from Link:

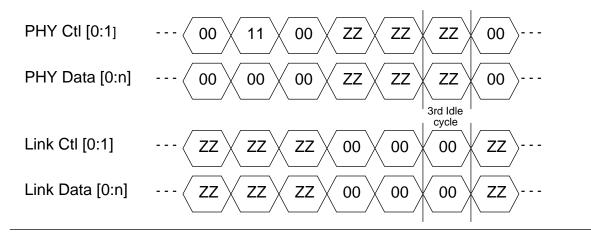


Figure 3: Link Cancel with at least 1 hold cycle driven by the Link: (note that this sequence is not described anywhere in P1394a)

PHY Ctl [0:1]	···· (00 11 00 ZZ)	 ZZ ZZ ZZ 00
PHY Data [0:n]	00 00 00 ZZ	 ZZ ZZ ZZ 00
	"hold"	"hold"
Link Ctl [0:1]	$\cdots \left\langle ZZ \right\rangle ZZ \left\rangle ZZ \right\rangle 01$	 $(01) (00) (ZZ) \cdots$

If the link wishes to release the interface without transferring any data, and it has driven at least one "hold" cycle, the link must follow the last "hold" character with 2 cycles of idle.