TO: P1394a Working Group

FROM: Steven Bard

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Alternate Power Providers (sometimes referred to as *Secondary Power Providers*) were intended to be able to provide some nominal amount of power to the cable when no other source of power is available. An Alternate Power Provider may or may not be capable of delivering the same quantity of power as a Standard Power Provider (sometimes referred to as a *Primary Power Provider*).

When a Standard Power Provider becomes attached to the bus, the Secondary Power Provider may discontinue providing power to the bus and behave as a normal self-powered multi-port node and pass power through.

Other implementations of Alternate Power Providers may desire to report a power capacity not available in the standard power_class field of one, two, or three but may require per port diode isolation due to a launch voltage conflict with a Standard Power Provider (e.g. it launches at 26 volts but delivers a power capacity of 10 watts)

The current draft specification (page 80, clause 7.3 paragraph three) reads:

"Power sources that identify themselves with POWER_CLASS of one, two, or three in their self-ID packet(s) shall implement, for each of their ports, the diode and current limiting scheme illustrated by figure 7-2."

This may be interpreted as precluding power class four nodes (Alternate Power Providers) from implementing per port diode isolation.

Text which expresses the same message as the original text (but not exclude Alternate Power Providers) may read:

"Power sources which deliver cable power at a voltage of 20 volts or more shall implement, for each of their ports, the diode and current limiting scheme illustrated by figure 7-2."

It is recommended that the suggested text be used in place of the original text (or at least a reasonable facsimile which delivers the same message).

The TPA/TPA* pair transmit the Strb_Tx signal and receive the Data_Rx, Arb_A_Rx and Speed_Rx signals. The TPB/TPB* pair transmits the Data_Tx and Speed_Tx signals and receives the Strb_Rx, Arb_B_Rx and Bias_Detect signals. The Strb_Tx, Data_Tx, Strb_Enable and Data_Enable signals are used together to generate the arbitration signals. The Arb_A_Rx and Arb_B_Rx signals are each generated by two comparators since they have three states: zero, one or high-impedance.

When enabled, the TPA/TPA* pair transmit TpBias while the TPB/TPB* pair receive the TpBias signal (this is used by the Bias_Detect comparator to determine presence or absence of TpBias). When TpBias is not generated, the connect detect circuit can detect the presence or absence of a peer PHY at the other end of a cable connection.

The bias generation circuit (including the external capacitor) shall be designed so that when TpBias is driven low, within 0.5 ms the capacitor shall be discharged and output bias shall be less than 0.1 V relative to VG. Contrariwise, when TpBias is generated the capacitor shall be recharged and the TPA/TPA* signals shall be within the specifications of table 4-14 of IEEE Std 1394-1995 within 1.0 ms.

NOTE—The current source used by the connect detect circuit, I_{CD}, shall not exceed 76 µA. This guarantees that the input to the peer PHY's bias detection circuit does not exceed 0.4 V.

7.3 Cable power and ground

This clause replaces 4.2.2.7 of IEEE Std 1394-1995, "Power and ground," in its entirety.

A node may be a power source, a power sink or neither and may assume different roles at different times. The principal method by which a node identifies its power class is the self-ID packet transmitted subsequent to a bus reset (see clause 7.5.1). There may be other facilities, for example in a node's configuration ROM, that identify the power characteristics of a node in more detail than is possible in the self-ID packet; these are beyond the scope of this standard.

Serial Bus may be unpowered or powered; in the latter case, there may be more than one power source. The possibility of multiple sources requires that power sources be manufactured such that current from a node providing higher voltage does not flow into sources of lower output voltage. Power sources that ~~identify themselves with POWER_CLASS of one, two or three in their self-ID packet(s)~~ provide a minimum output voltage of 20 V shall implement, for each of their ports, the diode and current limiting scheme illustrated by figure 7-2.

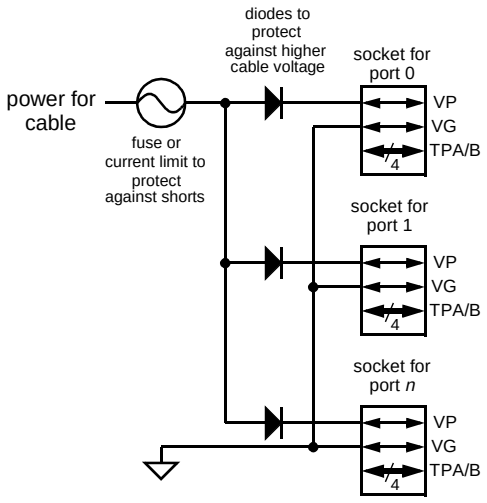

Figure 7-2 — Node power interface when VP is at least 20 V ~~for POWER_CLASS one, two or three~~