LPS

- 1394A (1.4) defines the LPS signal as "Link power status. Indicates that the link is powered and functional"
  - Link may not be truly functional until PHY has responded with SClk
  - LPS is also used to reset the PHY/Link interface
  - Update the definition - maybe it is just the "Link Phy Interface Signal. Used to control the PHY Link interface"

Missing POR text

During power-on reset, all outputs are held in high impedance until the operating mode (differentiated or undifferentiated) can be determined. If operating in undifferentiated mode, then some or all outputs may be taken to zero. All outputs not taken to zero shall be maintained in high impedance until the completion of POR.

Implementation means of setting configurable bits shall be sensed at the moment that power-on-reset completes. If operating in undifferentiated mode all outputs shall then be taken to zero.

Following a power reset or a PHY link interface reset, the link continues the initialization of the interface by asserting LPS. After observing LPS, the PHY
shall resume SClk (if necessary) within 2 SClk periods if it is asserting LinkOn, otherwise it shall resume SClk as soon as possible. If the interface is in differentiated mode, the PHY shall resume SClk by driving it low for half a SClk period.

No partial packets

- Upon the eighth SClk cycle the PHY shall assert Receive on Ctl[0:1] while simultaneously providing data prefix indication on D[0:n] for at least one SClk cycle. Upon the subsequent SClk cycles the PHY shall drive Ctl[0:1] and D[0:n] as follows:
  - the PHY shall continue to indicate data prefix while it is in a state in which it otherwise would be transferring data to the link, after which it shall assert Idle on Ctl[0:1];
  - no status information shall be transferred that commences part way through the status bits; and
  - no partial packets shall be transferred on D[0:n].

Propose deleting the third bullet, as it is covered in the first and adds confusion

PHY/Link DC Spec

- Editorial change

Name	Description	Condition	Unit	Minimum	Maximum
V_{LIT+}	Input rising threshold (LinkOn and LPS)		V		V_{LREF}+1 (b)
V_{LIT-}	Input falling threshold (LinkOn and LPS)		V	V_{LREF}+0.2 (b)	

Connect Detect on disabled ports

- Connection detect circuit shall remain active when a port is in P6:Disable.
  - necessary to choose between P5 and P0 on exit from P6:Disable
- Consider an intermitted (faulty) connection, sometimes setting bias, sometimes setting reset, etc. etc. - local port is disabled
  - When it sees a connection, the continuously running port monitor (Table 7-25 on p105) will set connection_in_progress. The reset_detected() boolean function may then detect a reset, and, because connection_in_progress is true, generate a reset.
    - ✓ This can be fixed in reset_detected().
- The continuously running connection monitor will still generate many disconnection notifications to the link
- Suggest remove any attempt to monitor the state of a disabled port
  - change the continuously running machine so that it does not look at bias or connect_detect if the port is disabled.
  - In addition, the end of disabled_actions() can wait for !disabled[i], and the transitions P6:P5 or P6:P0 can be selected on the value of connected[i].
  - Alternatively, always take P6:P5 - if there is no connection this will go to P0 pretty quickly anyway.
- Perhaps a disabled port should look as if it is disconnected anyway.

Decode PHY Packet

- decode_phy_packet() in Table 7-31 needs an additional branch at the end

```
else if (phy_pkt_.ext_type == 0xA)      // Remote confirmation packet?
     ;                                  // If so, ignore
```