

Texas Instruments, Inc.
IEEE 1394 Applications
Mixed Signal Products
Semiconductor Group
Dallas, TX 75243

FROM: Burke Henehan
TO: P1394a Ballot Response Committee
DATE: January 21, 1999
RE: Backplane PHY register set

I would like to propose that the register set for the backplane implementation of 1394 be standardized on the register set for the Texas Instruments TSB 14C01A as shown in this document. To my knowledge, Texas Instruments has the only implementation of a backplane PHY so this is the logical register set to standardize.

6.2 PHY register map (backplane environment)

The PHY register map for the backplane environment is related to that of the cable environment; some fields are not present and while other fields changeable in the cable environment have a fixed value in the backplane environment and *vice versa*. ~~In addition, the backplane environment may make use of the enhanced register map to indicate an enhanced register that contains the transceiver disable (TD) and Priority fields.~~

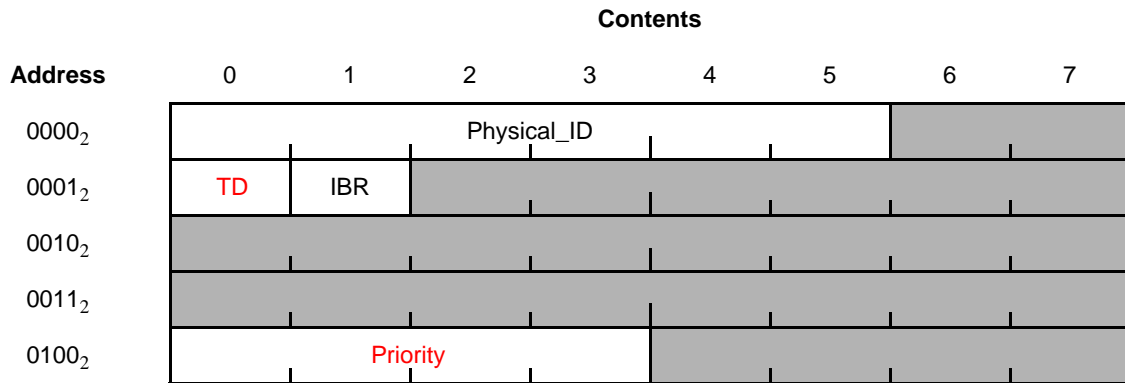


Figure 6-4 — PHY register map for the backplane environment

The meaning, encoding and usage of all the fields in the backplane PHY register map are summarized by table 6-4.

Table 6-4 — PHY register fields for the backplane environment

Field	Size	Type	Description
Physical_ID	6	rw	The address of this node; unlike the equivalent field in the cable environment, the physical ID in the backplane environment is writable.
TD	1	rw	Transceiver disable. When set to one the PHY shall set all bus outputs to a high-impedance state and ignore any link layer service actions that would require a change to this bus output state.
IBR	1	rw	Initiate bus reset. When set to one, instructs the PHY to initiate a bus reset immediately (without arbitration). This bit causes assertion of the reset signal for approximately 8 μs and is self-clearing.
E	1	r	If equal to zero, no enhanced registers are used. If equal to one, enhanced registers at address 0100₂ and 0101₂ are present.
Total_ports	5	r	The number of ports on this PHY. In the backplane environment there is one port per PHY.
AStat ₀	2	r	Data line state (uses the same encoding as for cable).
BStat ₀	2	r	Strobe line state (uses the same encoding as for cable).
ENV	2	r	Present if the E bit is one. ENV shall be equal to zero in the backplane environment; other values are reserved.
Reg_count	6	r	Present if the E bit is one, in which case it shall be greater than or equal to one. When Reg_count is greater than one, the format of additional enhanced registers at addresses 0110₂ and above are vendor dependent.
Priority	4	rw	This field shall contain the priority used in the urgent arbitration process and shall be transmitted as the <i>pri</i> field in the packet header.