LPS/LinkOn Duty Cycle

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Synopsis

Among the isolation barrier circuits for PHY-Link interface, the LPS and the LinkOn have the least marginal band from point of view of the DC specifications. Primary reason for this is their necessity for imbalanced bias point (i.e., the DC bias voltage on the receiver needs to be adequately lower than its input threshold so that an absence of pulsed signal will eventually be observed as a logical low by the receiver).
To improve the DC margin for this type of interface, a “duty cycle control” can be used. For example, assuming 25%Vdd bias (as it is illustrated in the informative circuits in clause 5.9.4), by having 25% duty cycle for the pulsed signal, a 75% of the total pulse height will appear above the bias voltage level. This way, the signal appears pretty much the same as “direct” CMOS interface and the DC margin issue can be greatly relaxed.
Unfortunately, however, LinkOn spec (table 5-4) does not allow the above scheme (it states minimum duty cycle for the LinkOn signal should be more than 40%). Although the LPS spec, on the other hand, does not forbid the “small duty cycle scheme”, it, at the same time, allows “large” duty cycle with which it is very likely to have a problem.
This document is made with the intention of eliminating unnecessary restriction (LinkOn) and avoiding problematic implementation (LPS) while providing a guidance to potential designers.

Recommended changes

In order to accommodate duty cycle control scheme, the next changes to the P1394a Draft 2.0 are suggested.

Table 5-2 LPS timing parameters (an excerpt)

Parameter	Description	Unit	Minimum	Maximum
T_{LPSL}	LPS low time (when pulsed)	us	0.09	1.00
T_{LPSH}	LPS high time (when pulsed)	us	0.09	1.00
	Duty cycle (when pulsed)	%	20	60

Table 5-4 LinkOn timing parameters (an excerpt)

Description	Unit	Minimum	Maximum
Frequency	MHz	4	8
Duty cycle	%	~~40~~ 30	60

Relationship between the duty cycle and the bias point

Figures below illustrate how the small duty cycle scheme (narrow “high” and wide “low”) improves DC margin.

As depicted in Fig.1, the imbalanced bias scheme is employed for the LPS and the LinkOn. The isolation circuits for LPS and LinkOn are basically identical, so we take the LPS as an example. If the Link (in this case) stops “pulsing” in any logical state, the voltage at the receiver’s end (the PHY in this case) finally settles at the bias voltage. Owing to its lower bias voltage, the PHY observes logical zero in this case. While providing the advantage of the usability of standard CMOS driver/receiver combination, it imposes a careful design consideration since the received high level of the signal only reaches 70 – 80% of the receiver’s Vdd. A supply voltage difference between the PHY and the Link makes the situation even worse.

Fig.2 illustrates the received signal waveform when the duty cycle is 50%.

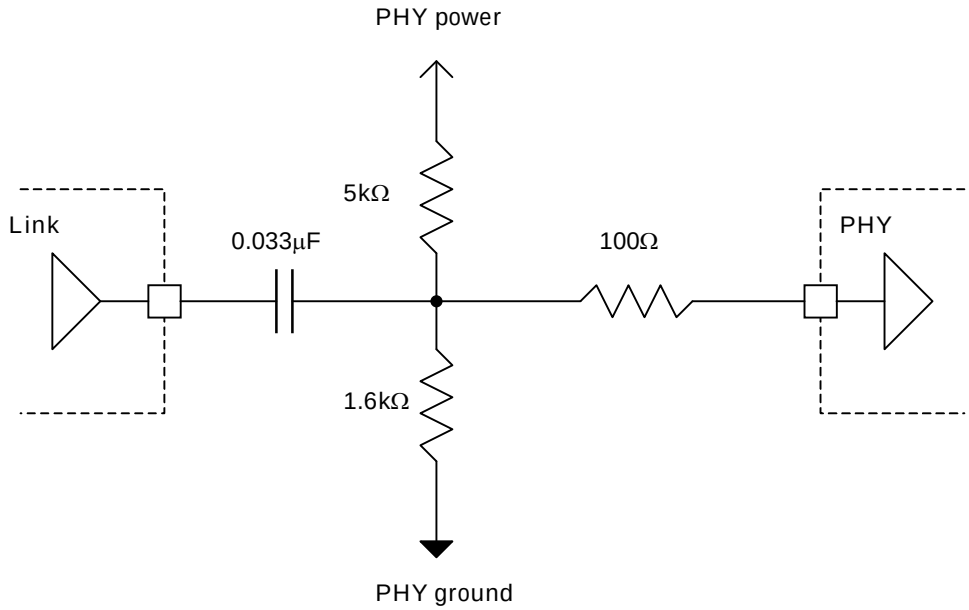

Fig. 1 Isolation circuit for LPS

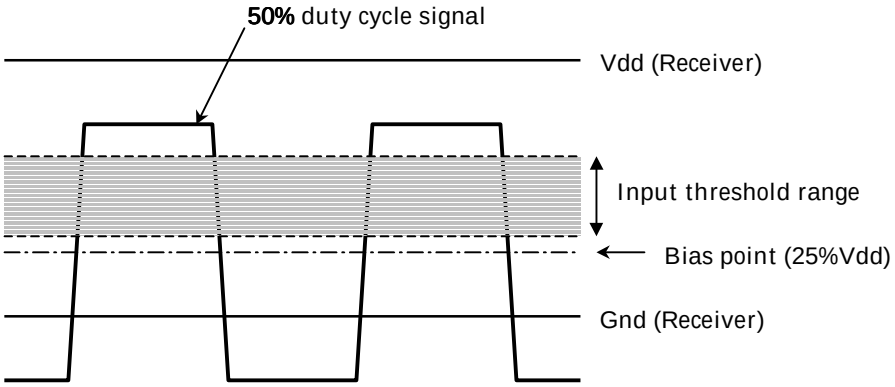

Fig. 2 Signal waveform at the receiver (**50%** duty cycle, in the steady state condition)

As depicted in Fig. 3, on the other hand, if the signal duty cycle is 25%, a 75% of the total pulse height appears above the bias voltage level. Assuming 25%Vdd bias (as illustrated), the received signal swings pretty much the same as direct CMOS interface (i.e., the high level reaches receiver's Vdd).

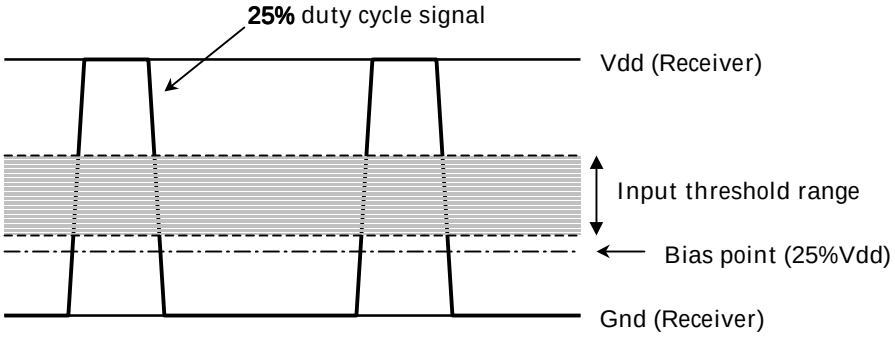

Fig. 3 Signal waveform at the receiver (**25%** duty cycle, in the steady state condition)

It is easily noticed that, if "large" duty cycle is used instead, the received signal tends to be even lower voltage. This implies that the DC margin for the logical high level would be eaten up.

In reality, however, an input ESD protector on the receiver "clips" the low level at somewhere around –0.5V. And this diode-clipping may prevent the signal from going negative further.
However, the protector circuit itself varies according to different silicon vendors. So it is difficult to rely on this. Besides, more importantly, a constant leak current flows through the diode during the low period of the cycle. And this implies an additional current consumption for the Link, and at the same time, it menaces the both chips (the PHY and the Link) with long term reliability failure. This, in turn, implies that board designers need to carefully choose a current limiting resistor (the 100Ω resistor in the example

circuit) according to the driver's output impedance.

Impacts on current designs

PLEASE NOTICE that this change may have an impact (very minor though) especially on a Link design. In short, the change requires Link implementation to be tolerant of LinkOn pulse width as short as 30% of 8 MHz cycle (i.e., 37.5 nsec) instead of conventional 40% of 8 MHz cycle (i.e., 50 nsec).
In accordance with the agreement in the BRC, the change will be in the revised draft unless there is any Link design which cannot adapt to the change. So reviews from Link designs are advised.