CONGRUENT SOFTWARE, INC.
98 Colorado Avenue
Berkeley, CA 94707
(510) 527-3926
(510) 527-3856 FAX

FROM: Peter Johansson

TO: IEEE P1394a Ballot Response Committee

DATE: May 10, 1999

RE: Backplane PHY register set

When Burke Henehan first proposed modifications to P1394a he suggested a writable bit in the same location as the *R* (root) bit in the cable PHY registers. The rationale was that some link designs will not function as a cycle master unless they read a value of one in this bit. Burke subsequently withdrew the suggestion because extant Texas Instruments silicon does not implement this bit.

I think the suggestion was worthwhile and offer the following proposal, that the bit be defined (in order that future implementations may provide this convenience in a standard way) but that its implementation be optional (in order to preserve compliance of existing silicon).

In addition, P1394a Draft 2.0 defines two fields, inherited from IEEE Std 1394-1995 annex J (informative) that are instantaneous representations of the backplane data and strobe line states. These are not implemented in Texas Instruments parts, but I think we should retain their definition but make them optional.

Other than these two modifications, the material that follows is identical with Burke s 99-001r0 submission.

6.2 PHY register map (backplane environment)

The PHY register map for the backplane environment is related to that of the cable environment; some fields are not present and while other fields changeable in the cable environment have a fixed value in the backplane environment and *vice versa*. ~~In addition, the backplane environment may make use of the enhanced register map to indicate an enhanced register that contains the transceiver disable (TD) and Priority fields.~~

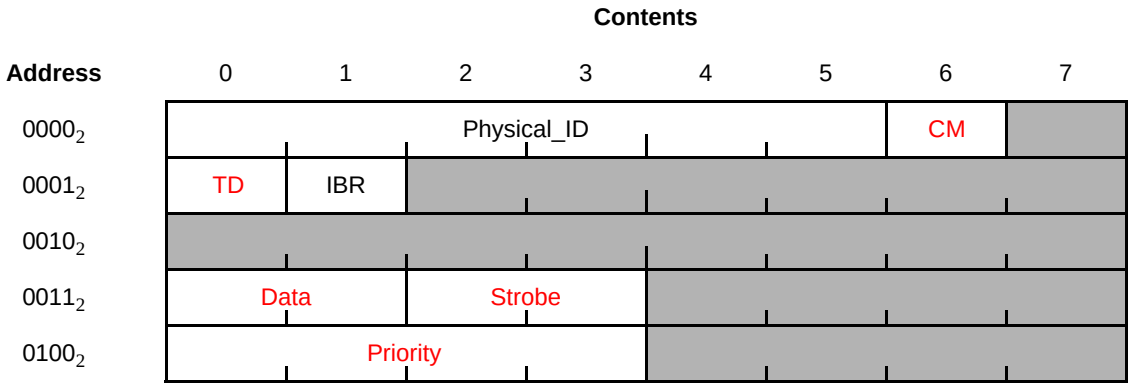

Figure 6-4 — PHY register map for the backplane environment

The meaning, encoding and usage of all the fields in the backplane PHY register map are summarized by table 6-4.

Table 6-4 — PHY register fields for the backplane environment

Field	Size	Type	Description
Physical_ID	6	rw	The address of this node; unlike the equivalent field in the cable environment, the physical ID in the backplane environment is writable.
CM	1	rw[a]	Cycle master. The value of this bit does not affect the operation of the PHY, it is present in the backplane PHY register map for the sake of compatibility with some link designs which do not operate as cycle master unless this bit is set to one.
TD	1	rw	Transceiver disable. When set to one the PHY shall set all bus outputs to a high-impedance state and ignore any link layer service actions that would require a change to this bus output state.
IBR	1	rw	Initiate bus reset. When set to one, instructs the PHY to initiate a bus reset immediately (without arbitration). This bit causes assertion of the reset signal for approximately 8 µs and is self-clearing.
~~E~~	~~1~~	~~r~~	~~If equal to zero, no enhanced registers are used. If equal to one, enhanced registers at address 0100_2 and 0101_2 are present.~~
~~Total_ports~~	~~5~~	~~r~~	~~The number of ports on this PHY. In the backplane environment there is one port per PHY.~~
Data	2	r	Data line state (uses the same encoding as for cable).[b]
Strobe	2	r	Strobe line state (uses the same encoding as for cable).[a]
~~ENV~~	~~2~~	~~r~~	~~Present if the E bit is one. ENV shall be equal to zero in the backplane environment; other values are reserved.~~
~~Reg_count~~	~~6~~	~~r~~	~~Present if the E bit is one, in which case it shall be greater than or equal to one. When Reg_count is greater than one, the format of additional enhanced registers at addresses 0110_2 and above are vendor dependent.~~
Priority	4	rw	This field shall contain the priority used in the urgent arbitration process and shall be transmitted as the pri field in the packet header.

[a.] It is permitted to implement CM as a read-only bit, in which case its value shall be zero.
[b.] The implementation of the Data and Strobe fields is optional; if unimplemented, these fields shall be zero.