

IEEE P1394a meeting
Honolulu, HI
August 4 - 5, 1997

Chair, Peter Johansson called the meeting to order at 8:45 am. The meeting started with introductions and then Peter presented the meeting agenda.

1. Introductions and procedures
2. Review of minutes
3. Old action items
 - 3.1 Single- and dual-phase retry protocol revalidation [Johansson]
 - 3.2 Multi-speed packet concatenation vs. token-style arbitration [Duckwall / Johansson]
 - 3.3 CPTWG letter [Johansson]
 - 3.4 Power distribution safety considerations [Busse]
 - 3.5 Link control of PHY acceleration [Murthy]
 - 3.6 DTDG notification of P1394a desiderata [Traw]
 - 3.7 PHY/link reset [Bennett / Hauck / Morrow]
 - 3.8 Update and publish SCAT [Whitby-Strevens]
 - 3.9 Legacy PHY acceleration issues [Eneboe]
 - 3.10 Bus request timings [Hauck]
4. Other old business
 - 4.1 Annex A
 - 4.2 Root contention timings
 - 4.3 PHY/link handover
 - 4.4 FAIRNESS_BUDGET
 - 4.5 Ping packet notification to link
 - 4.6 Alternate cable / connector (4-pin)
 - 4.7 Suspend / resume states for the PHY
 - 4.8 SClk availability
 - 4.9 PHY version registers
 - 4.10 PHY reset
 - 4.11 LReq (Timings, etc.)
 - 4.12 Cycle Sync LReq vs. accelerations
 - 4.13 Transaction code 0x0E
 - 4.14 Isochronous data packet tag
5. SCAT Review and Closure
6. New Business
 - 6.1 Security extensions [Brown]
 - 6.2 Redefinition of pwr_class in self-ID packets [Bard]
 - 6.3 Remote PHY register access [Bard]
 - 6.4 Electrical changes [Hannah]
 - 6.5 PHY timing constants
 - 6.6 Legacy PHY register map [Wooten]
 - 6.7 Self-ID problems (S100 vs. S400) [Fasano]
 - 6.8 SClk definition

- 6.9 PHY pinging constants [LaFollette]
- 6.10 Annex C (informative) [Wooten]
- 6.11 Vp relaxation [Wooten]
- 6.12 TP bias per port [Wooten]
- 6.13 Minimum cycle_offset in cycle start packet [Hauck]
- 6.14 Split timeout
- 6.15 Contender bit in self-ID packet
- 6.16 6-pin differential electrical performance [Brunker]
- 7. Meeting schedule
 - 7.1 Working group
 - September 25 - 26 (Boston, MA)
 - 7.2 Editorial sessions
 - September 24 (Boston, MA)
- 8. Review of action items
- 9. Adjournment

Minutes of the previous meeting unanimously accepted. David Wooten moved and Richard Churchill and seconded.

Old action items

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Carried over: 3.1, 3.2 and 3.9

Closed: 3.3, 3.6 and 3.8

Placed on the meeting agenda: 3.4, 3.5, 3.7 and 3.10

Annex A updates (Eric Hannah)

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Closed.

Root contention timing (Dave LaFollette)

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Dave gave a presentation on PHY root contention. The feedback he received was that it may not be applicable to 1394a but could be an issue with 1394b longer cables. For the longer cables, the cable delay could be too high for the root contention process to work properly. There was a question about the exact way to calculate cable delay using the current root contention constants. A question was asked as to what the max length of cable is that will be supported by 1394a and 1394b. Colin mentioned that cable lengths in P1394b could be much higher and covering P1394b cables with this constants may be problematic. So the issue is, "Should we set a max cable length for P1394a and/or change the constant to accommodate larger cable lengths?"

Straw Poll:

Do nothing 12
New times for copper DS encoding 25
New times for 1394b 3

Action item for PHY designers review to calculate the new root contention timing constant that is appropriate for a longer cable length on 1394a.

PHY-Link Handover: Extra idle cycle: (Colin Whitby-Strevens)
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This has to do with adding an extra idle cycle before the link starts driving the PHY-link bus after getting control from the PHY. This is a potential problem in the case where PHY-Link isolation is being used. One solution is to add an extra idle before the link starts driving the bus. Colin pointed out that as it is defined in the latest spec, this extra idle is optional. Another related issue is that if the PHY sees two idles it interprets that the link is giving up the bus. Colin pointed out that the PHY will see its own idle first and then the one sent by the Link. This means that if we connect a new link to an old PHY the old PHY may interpret this new idle cycle as a second idle cycle and think that the link wants to relinquish the bus and take over the bus.

Motion: Colin Whitby-Strevens moved and David Wooten seconded that the language in clause 5.1.4 of the July 30th draft be accepted.

The motion passed unanimously.

FAIRNESS_BUDGET: (Dave LaFollette)
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This was voted in the last meeting and the spec was modified to reflect this. Dave pointed out that there were some differences from his most recent proposal vs. what's in the new draft.

Field size: 4 bits vs. 8 bits for the field size.
Range Checking Responsibility: additional hardware range checking vs. checking done by bus manager
Total Requests Limitation: 63 vs. not defining (constraining) it in the spec.

Peter Johansson mentioned that it is a good thing to restrict the total of additional priority requests to no more than 63 minus the number of nodes.

MOTION:

Richard Churchill moved and Peter Johansson seconded that we adopt the language in clause 9.8 of the July 30th draft.

Discussion: Dave Wooten wanted the flexibility so that different application could configure the fairness depending on their environment. Peter mentioned that there was no evidence that having more than 10-12 more cycles per fairness interval added proportional benefits.

The motion passed 21:9:7.

Motion: Dave LaFollette moved and Peter Johansson seconded that the size of pri_req be changed to 6 bits.

Discussion: Dave Wooten and Jerry Hauck mentioned that 4 bits may not be adequate.

The motion passed 16:8:10.

Peter wanted to know if everyone wanted the pri_req and pri_pref fields to be byte aligned; the consensus was "Yes".

Range Checking Responsibility:

MOTION: Jerry Hauck moved and Peter Johansson seconded to change the draft so that the behavior is undefined when pri_req is written with a value larger than pri_pref.

The motion passed unanimously.

Ping packet notification + ping constants (Jerry Hauck)

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Dave LaFollette described the proposed timing constants required for PHY pinging. There was a lot of discussion on defining these new constants. Broadly, there were two different approaches that the group could agree with the new constants or have a mechanism to report these values by some software register bits. It was agreed that PING RESPONSE TIME should be a constant. In fact the PHY delay jitter was the only timing that the group thought would vary from node to node and should be something that should be reported by software means. Link to PHY delay: is this something that you

can find out by pinging yourself? Peter suggested that the PHY TO LINK DELAY and LINK TO PHY DELAY could have a maximum value that is agreeable to all PHY designers. Dave Wooten wanted to know if we could have a single jitter value per PHY that could be reported. He also mentioned that having constants with wide ranges between min and max don't give you an accurate information. Action Item: The consensus was that this we will review this issues in the next PHY designers review.

PHY Version Registers: (Peter Johansson)

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This proposal has to do with allowing a 24bit manufacturing vendor id based register space.

MOTION: John Fuller moved and Peter Johansson seconded that we adopt the proposal to add the version registers in the PHY register page as specified by 97-041r0.

Peter spoke against the motion and argued that it diluted pressures for PHY interoperability (at the software level) to uselessness.

Colin spoke for the proposal and said it was pragmatically necessary because of variations that already exist in PHY's from different vendors.

AMENDED MOTION: Peter Johansson offered an unfriendly amendment, seconded by Paul Levy, to define a vendor-dependent register page in lieu of John Fuller's proposal.

There was a considerable amount of discussion on this particular issue. One argument was that if a PHY vendor wanted to be a second source on an existing design then if there are some features that are not completely working and if we have some way of conveying this information to the software then the new design can be used in that board as is with the possibility of plugging in future releases of the chip.

David Wooten offered an amendment to the motion to include 1394 compliance level (P1394a vs. P1394b, etc.) in the register page. The amendment was rejected as unfriendly by Peter.

Colin Whitby-Strevens called the question. The unfriendly motion to amend failed 2:19:2.

Colin called the question on the original motion. The motion passed 10:8:10.

Tcode 0x0E:
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Tcode E is set aside never to be used in future since some current implementation are using it.

Tag == 1:
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Section 9.4 in the draft. When the tag equals 1 the format of the data field is specified by IEC 61883.

SCLK availability (Whitby-Strevens)
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This agenda item was moved to suspend/resume discussion. (availability of SCLK when all ports are turned off as well as when LPS comes up)

PHY reset: (Jerry Hauck, Neal Morrow)
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Jerry mentioned that if this is the only way to reset the PHY-Link then this wastes a pin on the link---but it is increasingly evident that the link LPS pin is going to be required for other reasons. Neal presented the need for the LPS reset feature and then its implementation.

Timing proposal: LPS active $T_{pwh} = 90 \text{ ns min}$ $T_{pwl} = 2.2.5 \text{ us max}$. (LPS oscillating input)

There was a lot of discussion on this point since it seems that the power management group is trying to use LPS for a different purpose.

MOTION: Colin Whitby-Strevens moved and Jim Skidmore seconded that Richard Baker's LPS proposal, 97-028r1, (including use of LPS to reset PHY link interface) be adopted for the draft. The timing details are **subject to confirmation**.

A question was raised about behavior if a bus reset occurs during the time that LPS is de-asserted by the link in order to reset the PHY link interface. Peter also asked if LPS was meant to be used for some other use as well? Dave Wooten responded that if the link turns off the LPS to turn off the SCLK, and then at some point in time all ports on the PHY get

suspended then the PHY core can get suspended as well (including the PLL's etc.) But after some discussion it was agreed that these two functions can be made to work in a compatible format.

Dave Wooten called the question on this motion. The motion passed 19:4:0.

One of the "No" votes objected on the grounds that only one SClk is available and that the behavior upon a bus reset while LPS is negated is problematical.

LReq table clarification (Colin Whitby-Strevens)

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Colin explained his new LReq table and timing diagrams. Only open issue was the impact of cycle synch request on a currently pending fair request. **Action Item:** Peter suggested that we add the text and diagrams to the spec subject to clarifications and subsequent vote from the larger group.

Cycle Synch LReq (Jerry Hauck)

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Jerry talked about some corner cases that he has discovered where cycle synch Lreq does not work. He explained two cases where a problem could potentially occur. In both cases the general problem is that the root node is not able to send the cycle start packet until a subaction gap is detected. However, the rest of the nodes recognize this subaction gap and enable their acceleration features thereby potentially causing the very problem that this feature is trying to prevent.

Jerry proposed the following solutions that had a varying degree of impact on current PHY and Link designs. The following table shows the proposal #, whether the proposal will change current Link and PHY designs and the description of the proposal.

#	Link	PHY	Comments
A	--	--	Don't solve the problem (statistically insignificant)
B	X	--	Link Abstention: (Non root link, after cycle synch, uses only immediate or isochronous until cycle start or reset gap.

B1	X	--	Link prevents concatenation / acceleration when cycle start is expected. For Fair and Priority requests, if the link receives a transmit indication from the PHY without getting an intervening subaction gap, the link (this means that the PHY is using acceleration) the link should relinquish the bus by sending two idle cycles to the PHY
C	X	X	Rename Cycle sync LReq (accelerate?) and add a new "decelerate" LREQ
D	--	X	Wait 2 subaction gaps to re-enable acceleration
E	X	--	Links directly toggles enable_accel???? Not sure if this will work work from a timing perspective and also might need a change in the PHY any way.

MOTION: John Fuller moved and David Wooten seconded that Option C be adopted.

Peter Johansson called the question and the motion passed 24:3:0. Jim Skidmore based his "No" vote on the objection that he will have to modify his current PHY design.

When acceleration bit is off the new cycle synch requests have no effect. 1100 is disable and 1101 is enable.

There was some discussion about the power up status of the enable_accel bit and the new hidden bit (controlled by the new LReq). Dave Wooten proposed that these bits be controlled independently by software. This was agreed by consensus.

SCAT Scope and closing actions table: Colin

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Colin presented a table containing all open action items. He reviewed each item and its status.

Isochronous Connection Management:

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MOTION: Dave Wooten moved and Peter Johansson seconded that section 8, " Isochronous connection management specifications", be deleted.

There was a lot of discussion on this subject: both for and against. Peter explained that section 8 adds additional speed bits for >= S800 and modifies the behavior of the IEC 61883 registers for devices not contemplated by the original, consumer electronic oriented work.

Jerry Hauck called the question. The motion passed 11:5:14.

More than 63 nodes:
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This is the case where the bus has more than 63 (max allowable) nodes. How does the user get notified.

Colin Whitby-Strevens moved and Peter Johansson seconded that a PHY shall not increment its 6-bit physical ID past 64. Software should treat reception of 63 as a bus configuration error and advise the user.

Richard Churchill called the question and the motion passed unanimously.

Action for the PHY designers review to describe and hash this.

Bus Info Block bootable device:
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Moved to IEEE 1212.

Arbitrated Short Reset Length:
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The length of the arbitrated short reset may not be long enough. This should be reevaluated during the PHY review.

Recommended way to set the local gap count:
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The PHY shall process and act upon the PHY configuration packet sent by its own link.

Formal definition of ACK packet for acceleration purposes
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If it is an 8 bit packet consider it to be an acknowledge packet.

Recommended interval between Software Initiated Bus Reset
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Action Item: John Fuller to write the text for and recommend where this explanation should be included.

Fairness Exemptions for Certain Devices (John Fuller)
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John Fuller moved and Steven Bard seconded to accept the proposal as written.

Peter spoke against the motion and asked how do you define disks, PC's and bridges. Neal also spoke against the motion.

The motion failed 2:18:0.

Speed rule checking proposal
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Whoever is initiating the concatenation should check and obey the rules. **Action:** Peter Johansson and Colin Whitby-Strevens to put the text in the next draft.

Force Root Timeout issue
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Will be reviewed at the next PHY designers review.

Suspend/Resume (Steve Bard)
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Steve gave an excellent presentation on the proposed suspend / resume protocol. He described the mechanism by which the bus manager can force various parts of a bus topology into and out of suspend state. More information on this protocol can be found in various documents at the power management ftp site: <ftp://ftp.p1394pm.org/pub/p1394pm/>

Annex A: Should it be normative?
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Consensus was that yes it should be.

4-pin connector (Dave Bruncker)
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There were some procedural issues about lack of more technical information and soft copies from the presenters from the last P1394a meeting in Bothell.

MOTION: David Wooten moved and John Fuller seconded that section 4, "Alternative cable media attachment specification", be removed from the draft.

Discussion: Peter J spoke against the motion. David Wooten mentioned that while the 6-pin connector is familiar to people and there is a base of empirical experience, he does not have enough information, at present, to vote to retain the 4-pin connector.

MOTION: David Wooten moved and John Fuller seconded that the motion to remove be tabled until the next P1394a meeting.

Discussion: Colin observed that we have had plenty of opportunity and time to provide this information. Peter Johansson also spoke against tabling the previous motion as by removing this motion seems to be the only means of getting more information on the 4 pin connector. Jim Busse spoke against the motion to table. Max Bassler spoke for this motion.

Richard Churchill called question; the motion to table passed 28:9:1.

Advocates of the 4-pin connector asked for some guidance as to what information is sought by the rest of the working group. The following section lists a request for information from Bill Prouty:

1. 'ALL' Japanese characters should be translated into English. Page 4 and 5 of the handout.
2. A summary of the data presented on page 6 Titled 'PC-7 Mass Production Unit'.
 - a. I would like to know if Peaked or Quasi-peaked.
 - b. At what angle were these measurements taken? Is there 8 sided scan data available?
 - c. What was the height and polarity of the antenna? Was it varied during the scan process?
 - d. What signals does Sony interpret as being contributed by the 1394 clocks, and or circuitry?
 - e. Have any tests been completed in a 10m chamber or 10m open range?
3. What is the correlation of the data on page 6 vs. page 7.

- a. Is it just the difference between prototype and production units? Do we care about prototype units if we do not know what the difference is between them?
- 4. Page 9. Could we get some pictures that are a little clearer so that we can better understand the setup?
- 5. Page 10. .
 - a. At what angle were these measurements taken? Is there 8 sided scan data available?
 - b. What was the height and polarity of the antenna? Was it varied during the scan process?
 - c. What frequencies does Sony interpret as being contributed by the 1394 clocks, and or circuitry?
 - d. Have any tests been completed in a 10m chamber or 10m open range?
 - e. What are we measuring? Cable tied to Ground, Chassis, bypassed, ??
- 6. Page 12. Would like clear pictures.
- 7. Page 13. Same questions as #2, and #5.
 - a. At what angle were these measurements taken? Is there 8 sided scan data available?
 - b. What was the height and polarity of the antenna? Was it varied during the scan process?
 - c. What signals does Sony interpret as being contributed by the 1394 clocks, and or circuitry?
 - d. Have any tests been completed in a 10m chamber or 10m open range?
 - e. What are we measuring? Cable tied to Ground, Chassis, bypassed, ??
- 8. Is there data available with just the Camera and just the VTR, and the Camera and VTR together?
- 9. General questions about the 4 pin Cable. Could it be connected to a device that has a green wire ground, or will all 4 pin devices be battery powered and / or isolated?

Some people suggested that the FCC submission itself would be very useful. David Wooten would like information on emissions characteristics when a 4-pin device is connected to another 4-pin device.

Suspend / Resume
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Straw poll on whether this discussion should be deferred to the next meeting in order to have more time to understand the proposal and have a more meaningful discussion.

The group decided to move on to new business and defer the suspend/resume discussion to next meeting.

Security Extensions: (Mike Brown)

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This issue has to do with getting legal opinion on the spoofing/snooping description language in the spec. Mike Brown has the **ACTION** to take it back to his legal group to get one more review. Paul Davies also took the **ACTION** to have this section reviewed by his company legal staff.

Power Management and Distribution: (Steve Bard)

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Steve explained the proposal that discusses the PHY power consumption. He explained that the maximum power consumption for a PHY is restricted to 3 W. Peter commented that it may be hazardous to using the current definition of power class (that means 1W) may be used by current power management software then this software may not work (or the bus may become overloaded if the software is setting the power class that used to be 1W but according to the new definition 3W)

Straw Poll on the impact on this proposal for increasing the power from 1W to 3W?

There was no conclusion as to whether this was a good idea or not. Peter Johansson suggested that we poll interested parties on the various reflectors and find out if they will be affected by this change.

MOTION: Peter Johansson moved and Colin Whitby-Strevens seconded that 97-032r0, as modified, be adopted for inclusion into P1394a. (The intent is to enable up to 3W of power consumption without a link on packet.)

The motion passed unanimously.

Peter Johansson, Steve Bard, and David Wooten have the **ACTION** to modify the document.

Electrical Changes: (Eric Hannah)

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Eric talked about his Spice models for the cable and connector and how they were derived. He also talked about some issues with DS signaling especially at S400 and proposed new rules on signal rise/fall times and receiver sensitivity for S400. Dave Wooten suggested that rather than tightening the spec on receiver sensitivity we should have text in the standard that will talk about the fact that this spec has no margin built into it.

Peter mentioned that item was both out of scope and that the proposed changes did not meet the two-week requirement.

Colin Whitby-Strevens moved and David Wooten seconded that the matter be brought within scope.

The motion passed 29:3:0.

Eric Hannah took the **ACTION** will put a document and his presentation onto the 1394a FTP site.

Meeting schedules

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Editorial session July 28-29 San Jose
Editorial session September 24 (Boston, MA)
Oct 22-24 (Maui, HI?)
Dec 3-5 (location to be determined)

Peter asked the group if electronic balloting on some non-controversial issues would be acceptable in the periods between working group meetings. This was accepted by consensus and will explore the possibility of doing this.

Legacy PHY register map: (David Wooten)

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Section 5.2.1 explains the legacy PHY register map. David pointed out that this need not be included in the P1394a standard.

David Wooten moved and Peter Johansson seconded that the legacy PHY register map be removed. Jerry Hauck called the question and the motion passed unanimously.

SCLK specification (Colin)

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Colin moved and John Fuller seconded that we accept the SClk specification on frequency and duty cycle as proposed by Colin in 97-045r0.

Jerry Hauck called the question and the motion passed unanimously.

Annex C (David Wooten)

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David pointed out that annex C section C.1 is in conflict with Annex A and could cause confusion. David moved and John Fuller seconded that the matter be brought within scope. There were no objections and it will be taken up at the next meeting.

Summary of Action Items:

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1. Calculate new root contention timing constants required for longer cable length. (PHY designers review group)
2. Review Ping timing constants at the next PHY designers review.
3. Add text from LREQ table into the draft, subject to clarifications and subsequent vote from the whole group. Peter Johansson
4. Review/clarify behavior when more than 63 nodes are detected during the initialization process. (PHY designers review group)
5. Add explanation to the draft regarding recommended intervals between software initiated bus resets.
6. Add speed rule checking text to the draft. Peter Johansson and Colin Whitby-Strevens.
7. Review "Security Extensions" text with internal legal groups. Paul Davies and Mike Brown.
8. Include 97-032r0, as modified, into the draft. Peter Johansson, Steve Bard, David Wooten.
9. Eric Hannah to post his "Electrical Changes" presentation and related documentation to the ftp site.

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