IEEE P1394a Working Group
January 16, 1997
Houston, TX

Acting chair Mike Sorna convened the working group meeting at 9:00 AM and indicated that the whole of the agenda was a detailed review of the first draft of P1394a, Draft 0.04. Mike substituted for the chair, Peter Johansson, until later in the morning.

CONNECTORS and CABLES

A task group comprised of industry representatives and led by Max Bassler contributed the material in section 4 of the draft standard. This group, principally connector and cable manufacturers, had met separately to refine the drawings and technical specifications.

Max led the working group in a review and discussion of the material in section 4, “Alternative cable media attachment specification.” The discussion was lively and a number of concerns were raised:

- Existing 4-conductor cables have been manufactured without individual shielding for the signal pairs. This may preclude the reliable use of these cables at faster speeds such as S200 or S400. Additional shielding could raise the cost of the assembled cable by 20% to 25%, according to Max’s estimate.

- If there are to be standards for two distinct 4-conductor cable constructions, each with its own speed rating, how would the cable be distinguished? Color coding? How much end-user confusion would arise and how would it affect the market?

- Will the unshielded cables pass FCC tests for emitted radiation? Will they pass when connected to other equipment, such as a computer system?

The working group agreed that the discussion was hampered by lack of quantitative data. Mike Brown agreed to conduct EMI tests with the available Sony 4-conductor cables in both the 4-pin and the 4-pin to 6-pin connector configurations.

Max invited proposals and asked that they be available for the next task group meeting (to be announced by Max).

PHY/LINK INTERFACE

Rich Mourn had provided the material in section 5, “PHY/Link interface specification,” and lead a review and discussion. The bulk of the material in this section was taken from (informative) Annex J in IEEE Std 1394-1995.

Rich pointed out the following changes:

- Speed encoding increased from two bits to three bits in anticipation of the P1394b high-speed PHY extensions.

- Two new bus requests by the Link, accelerated fair and accelerated priority request, were added to the LReq interface. (NOTE: Discussions later in the day rendered these unnecessary)

- A “paged” style of access to PHY registers which should provide ample extension to the current (very limited) address space of 16 PHY registers.

- A protocol to indicate different speed codes for each of a sequence of concatenated, transmitted packets.

- General purpose PHY interrupt defined to signal software to refresh information from all PHY registers.

The updated PHY register map is NOT reflected in Draft 0.04. At present it is available in a separate document, PHYReg.pdf, at the FTP site (see below). The editor is expected to incorporate the changes into the next draft of P1394a.

PHY ENHANCEMENTS

Bill Duckwall has written a white paper on numerous enhancements to the PHY; it is available as Duckwall.pdf on the FTP site, ftp.symbios.com:/pub/standards/io/1394. The material in the white paper is the technical foundation of section 6 , “Cable physical layer performance enhancement specifications” in the draft standard.

Bill conducted a review and discussion of the enhancements. The principal elements are summarized below:

- Connection/disconnection hysteresis

- Arbitrated (short) bus reset

- PHY “pinging”

- Accelerated arbitration (after an ACK or “fly-by”)

- Token-style arbitration

- Multi-speed packet concatenation

- Incremental topology reconfiguration without bus reset

There was detailed discussion of these PHY topics until the conclusion of the meeting. Unless a conclusion was reached which differs from the draft standard, the details are not given below. Because we ran out of time, the working group didn’t get to discuss: token-style arbitration, per port disconnect (controllable by software) or incremental bus reconfiguration.

CONNECTION HYSTERESIS

With respect to connection hysteresis, Bill had proposed a timer for each port of an N-port PHY in order to time an interval while a new connection becomes stable. It is possible to use a single timer for all PHY's; the drawback is that the initiation of a connection on a PHY while a time-out period is already underway on another will extend the time-out for the first. The working group agreed that this is an unlikely occurrence and that a single timer is adequate. The corrected state diagrams and C code will reflect the change.

PHY "PINGING"

A lengthy discussion of "pinging" followed. The PHY "pinging" facility provides a way to measure 1394 transmission delay times when cables longer than 4.5 meters are used or non-standard transmission media (repeaters) are used. The chief concerns about PHY pinging involve how much complexity to add to new PHY's in order to best support Serial Bus configurations with a mixture of new and old PHY's. The consensus reached was:

- All new PHY's shall respond to a "ping" packet by transmitting their self-ID packet

- The ability to time a "ping" packet is an OPTIONAL P1394a facility

- The facility for remote PHY "pinging" was dropped.

- Bus manager-capable nodes SHOULD be implemented with new PHY's that have ping timers. If not, they may be unable to optimize gap count in a Serial Bus with a mixture of new and old PHY's.

MULTI-SPEED CONCATENATED PACKETS

Bill then explained that the concatenation of packets at different speeds was not prohibited by IEEE Std 1394-1995 but was hampered by ambiguities in the current standard that MIGHT result in interoperability problems between PHY's when we extend the standard. Bill asked that silicon vendors research the following and provide answers at the next meeting:

- When an S200 packet is concatenated to another S200 packet, do PHY's send a speed signal for the second packet?

- In the same situation, but in the case of a receiving PHY, if no speed signal is received for the second packet, at what speed is it received?

ARBITRATED (SHORT) RESET

Bill advised the group that the proposed 1.3 us duration for arbitrated (short) resets had been chosen with “reasonable” cable lengths of up to 100 meters in mind. If the group had expectations that future use of 1394 might push past this limit, perhaps we should consider a longer duration? After discussion, 1.3 us was considered sufficient.

ACCELERATED ARBITRATION

After an explanation of ACK accelerated arbitration, Hisato Shima observed that there could be a problem. Under some circumstances, the root could not be guaranteed bus availability in time to transmit the cycle start.

The working group devised an alternate method:

- PHY’s that support accelerated arbitration shall also have this feature enabled by a bit in a PHY register.

- A new request type, cycle start, is necessary for the LReq interface from the link to the PHY. The link asserts this request each time its free-running cycle timer counts a new 125 us interval.

- From the time that the PHY receives a cycle sync request to the time that a subaction gap is observed on the bus, the PHY shall not utilize any arbitration acceleration tricks---neither ACK accelerated arbitration nor “fly-by” arbitration.

- At all other times, the PHY is permitted to use accelerated arbitration if this feature has been enabled by software.

A fringe benefit of this approach is that the proposed new LReq request types, accelerated fair request and accelerated priority request, are no longer necessary. The PHY may automatically determine whether or not accelerated techniques are usable.

ACTION ITEMS

- Mike Brown to report EMI test results for 4-pin cables.

- Bill Duckwall and Peter Johansson to develop accurate state diagrams for PHY arbitration states that reflect the proposed enhancements.

- Silicon vendors to research contemporary PHY implementations to answer the questions raised about multi-speed packet concatenation.

- Peter Johansson (editor) to incorporate available changes into a draft revision to be available at the end of January.

MEETING SCHEDULE

The working group discussed and tentatively agreed to the following schedule:

February 5 - 6, 1997 (Wednesday - Thursday)
Redmond, WA

March 17 - 18, 1997 (Monday - Tuesday)
San Jose, CA

April 16, 1997 (Thursday)
Eindhoven, Netherlands
Dependent upon expected turnout, this could be a two day meeting

May 6 - 7, 1997 (Tuesday - Wednesday)
Natick, MA
P1394b is expected to meet in Natick the same week

NOTE: The schedule above reflects a change, February 5 - 6, from the dates actually discussed in Houston.

CONCLUSION

These meeting minutes were compiled from notes taken by Lou Fasano and Diana Klashman and from the writer’s memory. P1394a is in need of a volunteer for the position of Secretary, since we stand to lose our current secretary, Dick Scheel, to schedule conflicts.

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Chair, IEEE P1394a

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