IEEE 1394A Working Group Meeting
Embassy Suites, Tempe, AZ
May 20-21, 1997

The working group would like to thank Intel Corporation for hosting this meeting. Also the secretary wishes to thank Jerry Hauck for taking the minutes for the second day of the meeting. The meeting started at 8:30 am with introductions. The minutes of the previous meeting were approved as written. Chair, Peter Johansson, started with the following agenda:

Agenda

1. Introductions and procedures
2. Review of minutes
3. Old action items
   - 3.1. Single- and dual-phase retry protocol revalidation [Johansson]
   - 3.2. Impact of multi-speed packet concatenation on token-style arbitration [Duckwall / Johansson]
   - 3.3. Cable / connector test procedures [Hannah]
   - 3.4. CPTWG letter [Johansson]
   - 3.5. PHY-Link interoperability [Kanhere]
   - 3.6. Direct connection drawing [Wooten]
   - 3.7. Link stop bits [Johansson]
   - 3.8. June meeting location [Fuller]
4. Other old business
   - 4.1. Annex A
   - 4.2. PHY reset via LPS
   - 4.3. Near-end cross talk
   - 4.4. OpenHCI desiderata
   - 4.5. Fairness optimizations
   - 4.6. Suspend / resume states for the PHY
   - 4.7. Asynchronous streams
   - 4.8. Loop detection and healing
   - 4.9. Power distribution
   - 4.10. AC timing constants
   - 4.11. LReq stop bits
5. New Business
   - 5.1. Link request table [Bennett]
   - 5.2. PHY/LINK transmit timings [Hasegawa]
   - 5.3. Data length in request / response [Johansson]
   - 5.4. Data length and max_rec [Johansson]
   - 5.5. SClk availability
   - 5.6. Alternate cable / connector [Churchill]
   - 5.7. Caboose packet and legacy PHY's [Newman]
   - 5.8. PHY pinging [Hauck]
   - 5.9. Draft 0.08 review

6. Freeze of document scope

7. Meeting schedule

   7.1. Working group
   June 24 - 25 (Bothell, WA)
   August 4 - 5 (Honolulu, HI)
   September (location TBD)

   7.2. Editorial sessions
   July 28 - 29 (San Jose, CA)

8. Review of action items

9. Adjournment

Peter reviewed the old action items and noted that items 3.5, 3.7 and 3.8 are now complete.

Annex A: Isolation: 1394A spec should make the section on Isolation informative v/s normative:
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A straw poll was taken to see if 1394A spec should simply state that “Annex A in IEEE 1394-1995 standard is optional” and whether this would be sufficient to convey our intent. There were no votes FOR and several AGAINST this idea and the consensus was to edit the relevant sections in the current spec and also to have a separate section on isolation in the 1394A specification.

Eric Hannah described his proposal that he had presented in our March meeting. He took the action item to send specific edits in a Frame Maker document to Peter Johansson.

PHY - Link interface reset via LPS:
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This discussion centered on finding a way to reset the PHY-link interface to a known state. There are certain conditions under which this interface may go into an unknown state. One of the conditions cited by Jim Skidmore was the case when the link is transmitting a packet and in the middle of transmission it gets a software reset from the host. The link responds to this reset by clearing its state (including the PHY link interface state machine) but the PHY continues to be in the transmit mode. This means that no one is driving the data and control pins on the PHY-Link interface and this may cause the PHY state machine to hang in certain implementations. One proposed solution was to use LPS to reset this interface. When LPS is driven inactive, the PHY-Link interface will get reset. Also, Jim Skidmore commented that if the state timeouts are enforced by the PHY then the PHY should eventually come out of transmit state and start driving the PHY-link interface again. Another proposal was to have a register bit that could be set by LREQ.

A straw poll was taken on some of the possible solutions:

1. LPS Yes 1
2. Enforcing Time-out Yes 7
3. New LREQ Yes 0
4. New reg bit: Yes 4

Rich Baker took the action to a) come up with the problem definition and b) describe how the proposed LPS scheme will work.

Cable/Connector Test procedures: Eric Hannah:
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Carried over to next meeting

Near end cross talk:
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Carried over. No one was available to speak on this topic.

Power distribution: Dave Wooten
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Dave talked about safety issues involved in supplying power over the cable. He presented the IEC950 and UL requirements for current limiting. The current 1394 spec does not have a similar spec. He explained various current limiting schemes for different configurations. He will post his proposal on the reflector and also took the action to send the text for the draft to Peter Johansson.

Open HCI desiderata
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Peter asked if the current draft for 1394A covers the ‘wish list’ for the Open Host Controller Interface. John Fuller had some questions on configuration ROM ‘generation’ bit (bus_info_block). There was some discussion on the generation bit and software reset and it was pointed out that some clarifications may be required in the draft. Peter took the action to include these in the draft.

Cycle lost prediction. Jerry Hauck
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Carried over to next meeting.

Copyright Protection proposals:
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Brendan Traw told the group that the CPTWG currently had 7 different proposals under discussion. He took the action to summarize the current proposals and put them on the reflector by first week of June.

Loop detection and healing:
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No proposal was submitted on this topic and consequently this item has been taken off the active list.

Asynchronous Streams:
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Peter Johansson explained the concept of asynchronous streams and how it could be used to transport IP over 1394 using tcode ‘A’. This feature requires the so called “loose isochronous” mode where the link is required to accept tcode A packets when in the asynchronous state. OHCI supports only loose isochronous operation. Peter explained that for current implementations, isochronous time may be used by allocating bandwidth and channel(s) for this purpose thereby allowing software infrastructure to be built to accommodate the IP broadcast.

John Fuller moved and Dave Wooten seconded a motion requesting the editor to add the asynchronous stream operation to 1394A draft.

The motion passed without discussion with 12 Yes votes, 0 No votes and 4 abstentions.

Stop Bits:

Jim Skidmore mentioned that some Link implementations do indeed send back to back Link requests with only one stop bit in between. After some discussion, the conclusion was that 1394A PHYs shall recognize both 7 bit and 8 bit requests.

Phy-Link Transmit timings: Yasumasa Hasegawa

Hasegawa explained the need for an additional idle cycle when the control is transferred from the PHY to the link during a transmit operation. The extra idle cycle is needed to avoid contention on the control pins when the link starts driving either 01 (wait) or 10 (transmit) and the PHY continues to drive 00 for a short period of time before its buffers are tri-stated. The consensus was to add this extra idle cycle for 1394A implementations of PHYs and Links. In order to ensure compatibility with older links, the 1394A phys should accept both the old and the new link behavior.

Data Length in Request/Response: Peter Johansson

Does the read response length have to match with the same length requested? Consensus was that yes the lengths have to match. So send either a 0 length packet with error response code or requested length with normal response code.

Data Length and Max Request: Peter Johansson

The maximum size of a block write request is currently specified by max_rec in the configuration ROM bus information block. How can applications determine the related maximum size for a block read request? Trial and error? Or should the max_rec field be redefined to specify both? No conclusion was reached.

SCLK availability:

There was some discussion on when SCLK was driven by the PHY. Some implementations tri-state SCLK signal if LPS is inactive and some others continue to provide SCLK when LPS is inactive. In some cases the PHY goes into sleep mode when all its ports are unconnected regardless of LPS. In this case, for this particular implementation, all signals on the PHY link interface will be tri-stated except for SCLK. There was some discussion on autonomous power-down modes and problems associated with this behavior. Claude Cruz mentioned that we should be careful with autonomous power downs. Jerry Hauck mentioned that we should consider the interaction between autonomous power down and the new per-port software disconnect feature. Also, in case the PHY goes into auto-power-down mode, the link won’t be able to read the PHY registers? The consensus seemed to be that the PHY should power down only if the link wants it to. There was no conclusion on this topic and some more discussion on the reflector is warranted.

PHY-Link interface corner case: Prashant Kanhere

Prashant presented a corner case in which a PHY may not be able to send a subaction gap to the link. The scenario is as follows:

1. The PHY has just entered the idle state and its arb counter is counting up to the subaction gap.
2. Just before the subaction gap is detected, the link completes a register read request and the PHY starts a status transfer by sending the first two status bits (arb reset gap and subaction gap bits). Since the subaction gap has not been detected yet, this bit will be zero.
3. Subsequent to above, the PHY detects the subaction gap.
4. The register request takes 8 SCLKs (160 ns). Before this is complete, another node, having won the arbitration, starts transmitting a packet. This PHY, upon sensing Data_Prefix, terminates the status/register read transfer and asserts RECEIVE on the control lines of the PHY link interface. At the same time it also clears the subaction gap bit since this condition is not valid any longer. Thus this subaction gap will never be sent to the link.

Things get even more interesting if prior to the recognizing the subaction gap the bus was in the isochronous phase. In this case, the received packet will be an asynch packet. However, since the link never received the subaction gap indication, it remains in the isochronous state. Thus it will receive a asynch packet in isochronous state. Further more, if the new asynch packet is aimed at this node, the link will not be able to send an acknowledge back since it is still in the asynch mode. After a lot of discussion and several alternatives later, Neil Morrow suggested that a 1394A PHY should defer servicing a read register request from the link during a timing window (to be defined) before the detection of the subaction gap. This will ensure that when the read is actually serviced, the status bits will include the subaction gap event indication as well. Prashant took the action to send the definition of this new rule to the editor.

Continued Discussion of "Fairness Optimization"

Richard Churchill and Dave LaFollette debated the merits of fairness optimization and field questions on their independent proposals. A few observations (but not exhaustive) offered during the discussion: Churchill's proposal allows a small constant number of cheats per fairness interval while LaFollette's ensures that the sum of the cheats and fair subactions per interval doesn't exceed 63. From this, it was argued that the former proposal benefits large configurations with many devices since the cheats can be dynamically shared among nodes while the latter proposal benefits small configurations when each device could be awarded a larger number of cheats.

Also it was noted that the Churchill proposal did not provide a deterministic method to tune accesses for a specific device while the LaFollette proposal required initialization by the bus manager to affect any improvement. The Churchill proposal is complicated by speed domains while the LaFollette proposal

exposes another opportunity for errant software to adversely affect bus performance.

The group was unable to achieve consensus on either the need for or the impact of arbitration cheats. Some workgroup members felt that the performance data justified addition of the optional feature while others felt peer review had not been sufficient. As a further uncertainty, P1394b may have the opportunity (via full duplex links) to enhance arbitration and hide many of the timing gaps. A straw poll passed by majority requesting that we defer any action until the June meeting, that critical peer review be solicited via the reflector, and that proposed P1394b arbitration enhancements be reviewed for potential impact.

Continued Discussion on PHY/LINK Timings

An ad hoc subgroup met Tuesday evening to establish and revise necessary PHY/Link interface timing specifications. Colin reported back that the subgroup reached tentative closure on the AC timings. Three tables were created: AC timings at the PHY, AC timings at the LINK, and general AC timing parameters. One noteworthy change reduced the delay through isolation from 3 ns to 2 ns, returning some of the budget to the LINK and PHY. A question regarding potential contention when the bus ownership changes from LINK to PHY and vice versa remains to be addressed. Otherwise, the AC specifications are considered solid and ready for final review.

The subgroup also identified the need for DC parameters as well. Colin distributed a draft of the necessary specifications which were largely borrowed from similar standards. Significant review of this first draft will be required before the June meeting.

Given the limited time remaining before letter ballot, Colin set the expectation that if no comment is posted to the reflector before the June meeting, then the proposed AC and DC specifications will stand as ratified.

Alternative Cable/Connector Discussion

The working group expressed concern that although EMI testing of the alternative cable/connector has been conducted by at least one company, results have not been forthcoming for various reasons including threats of legal reprisal. Without sufficient opportunity for critical peer review, the workgroup is unable to seriously endorse the alternative cable and connector. Consequently, Richard Churchill moved and John Fuller seconded that Section 4, the 4-pin connector specification, shall be removed from the P1394a draft standard unless sufficient data is presented by the end of the P1394a Working Group meeting on June 24 - 25, 1997.

The motion passed 16:1 (no count was made of abstentions).

Power Management Proposal Update and Liaison Report

The Power management proposal discussion was led by Claude Cruz with brief liaison reports from section experts. Highlights

include a review of the P1394a pertinent power management states: standby and suspend. Standby requires a node to respond (without awaking) to reads of the bus info block and isochronous resource management registers. Any other requests can be given an ack_tardy and should initiate a wake-up to the node. Suspend is defined on a per segment basis (between two adjacent PHY's) and will require a PHY level wake-up mechanism potentially based on TPBIAS. It was noted that the use of TPBIAS may have impact on fiber optic solutions (no DC path) or P1394b plans to use TPBIAS for startup signaling.

The power distribution liaison report outlined new definitions for power providers, consumers, etc. While the new definitions represent consensus of a small ad hoc task group, review with the full power management audience is anticipated at the 6/12 -6/13 power management meeting. Further details will be announced on the Power Managers reflector (list@p1394pm.org). To subscribe, E-Mail your name and the name of the company you represent to: steve_bard@ccm.jf.intel.com.

To facilitate forward progress on P1394a, the power management group will develop two lists: 1) specific changes required against IEEE1394-1995, and 2) recommended enhancements for inclusion in P1394a.

Freeze of Document Scope

Richard Churchill offered the motion, "Peter Johansson to publish current scope of P1394a to the reflector and the published scope will stand unless objections received within 5 days." Seconded by Steve Bard. A friendly amendment to extend window to 7 days was rejected. A second friendly amendment by Peter Johansson was accepted stating "Subsequently reopening the scope requires 2/3 majority of voting members present." The amended motion carries unanimously (17-0).

2 Week New Business Rule

The Chair, Peter Johansson suggested that the working group adopt a "2 week rule". Richard Churchill moves (with friendly amendment) "If new business is introduced at any meeting for which no advertisement or substantiating documentation was posted at least 2 weeks in advance, then no action will be taken on the new business." Mike Brown seconded the motion which carried unanimously.

Possible Bristol Meeting Site

Colin Whitby-Strevens obtained hotel rates for a proposed September meeting in Bristol. The Drury Hotel will provide rooms at 110 pounds per night which includes a meeting room for 40.

Liaison with DAVIC

The chair received a letter from the President of DAVIC encouraging the creation of a formal liaison between DAVIC and

IEEE (P1394a). Bradley Saunders moved for the establishment of a liaison with DAVIC with particular emphasis on matters of IP over 1394 and home networking. John Nels Fuller seconded and the motion carried unanimously.

Question on Forward Referencing Specifications

A question from the floor highlighted that the P1394a draft provides speed encodings for speeds which are not defined anywhere else in the specification (e.g., S800, etc.). The chair offered that it is acceptable to forward reference other draft specifications, and Colin Whitby-Strevens indicated that the proposed speeds for P1394b are considered stable. Action item for the editor to add a reference to P1394b.

P1394b Liaison Report

Colin Whitby-Strevens provided the liaison report. The P1394b scope was extended to encompass support for long distance media and coding. Two task groups were formed to look at the physical media dependent (PMD) aspects of long haul. The first group, chaired by Taka Fujimori and known as "low cost, low cost, low cost", will focus primarily on S100 over 50-100m of UTP CAT 5 or plastic optical fiber. Colin Whitby-Strevens will chair the "high speed, low cost, low cost" group with focus on long distance solutions for S800 and higher. One goal is to encourage home installations to choose media which will support these higher rates. Impacts to P1394a may include the need to specify or determine longer PHY delays and to determine speed capabilities of the actual media. P1394b expects to see first silicon in early '98 with a final standard sometime in the second half of '98.

Legacy Impact of Caboose Packets

Merril Newman discussed the impact the proposed P1394a caboose packets can have on some currently shipping 1394 silicon and devices. Some implementations which want to become the IRM snoop self-ID packets during a self-ID phase and apply the consistency checks outlined in section 8.4.2.3 of the 1995 standard. However, in performing these consistency checks, the extended self-ID packet sequence number "n" is ignored and assumed to be 0, 1, or 2. In direct contradiction with Table 4-29, these implementations will not recognize the n=7 sequence number for the P1394a caboose packet and will incorrectly interpret the contents of the caboose packet. The only identified failure mode is when the root device sends a caboose packet and, while applying the last consistency check of 8.4.2.3, older 1394 devices incorrectly determine that the last self-id packet set lists a port connected to a parent.

A few solutions were discussed including a proposal that only S800 and above PHY's send caboose packets, thus limiting the exposure of the older devices until S800 arrives. Before the solutions were fully evaluated, Richard Churchill moved that the interoperability issue between the new caboose packet and older consumer devices be noted in the minutes, and that evaluation of

solutions be moved to the reflector and the next meeting. John Nels Fuller seconded the motion which passed unanimously.

Presentation of LREQ Table

Joe Bennett proposed a table which clearly documents the conditions under which an LREQ can be issued by the link to the PHY as well as the conditions under which the PHY will abort or queue the corresponding LREQ. On suggestion of the editor, Joe will clean up the table to clearly differentiate LINK actions from PHY actions. One clarification to the proposed table included that an ISO request can be issued by the PHY only when the PHY/LINK interfaces is in transmit or receive. Thus, nodes with isochronous packets to send must first request the PHY while the cycle start packet is being received (slaves) or sent (master). This restriction also ensures that a late arriving ISO requests doesn't "pass" a subaction status indication from the PHY.

As part of the discussion, the group agreed that a cycle master shall not send a cycle synch LREQ to it's PHY. This helps ensure that after an internal cycle sync event, the cycle master can immediately request the bus and win arbitration for the cycle start packet before cycle slave PHY's revert back to accelerated arbitration with the arrival of a subaction gap.

Chapter 5 Clarifications

Ganesh Murthy presented some requests for editorial fixes and clarifications in Chapter 5. Two items were addressed by the LREQ table discussion above. A third item clarified that MAX_BUS_HOLD is enforced by the link design rather than the PHY. During concatenation, the PHY enforces MIN_PACKET_SEPARATION when the link drives the interface idle after asserting hold for one clock. Upon a subsequent grant from the PHY, the link may drive hold until data is ready or until the link chooses to gracefully terminate with a null packet by returning the control state to IDLE.

A lively discussion about whether ack-accelerated arbitration could always be enabled ensued, but was quickly answered by a note in Bill Duckwall's original enhancement paper noting a legacy compatibility issue which requires ack-acceleration to be disabled around cycle synch events. (Jerry Hauck and Ganesh Murthy have an action item to clean up the confusion they caused via the reflector.)

Since a link must send cycle sync LREQ's to a PHY in order to properly enable arbitration enhancements, it was noted that asynchronous only devices must still implement a cycle timer to benefit from the accelerations. For links (legacy or otherwise) which do not have a cycle timer, the default power-up state of the PHY with respect to enabling enhancements is important. (Enhancements should not be enabled for links with no cycle timer unless no cycle master exists.) These issues are expected to be clarified by Jerry and Ganesh over the reflector as well.

Additional PHY/LINK signals were discussed and the following

consensus reached for inclusion in the P1394a specification:

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 CLK25: not useful for the cable environment
   LPS: optional on link, required on PHY
LinkOn: optional on link, required on PHY
Direct: optional on link, required on PHY
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Phy Pinging

Jerry Hauck repeated a presentation on PHY pinging given in Eindhoven. The goal of PHY pinging is to provide a dynamic method to determine optimal gap count settings for long distance topologies. There appeared to be consensus that new PHY's will respond to ping packets and that a single timer in the bus manager will be used to calculate end-to-end cable delays. Implementing the timer in the link of the bus manager rather than the PHY has the added advantage that older PHY's could be "pinged" by timing the return of an ack from a normal asynchronous request to the legacy device. Determining gap count from a single timer also requires additional PHY_DELAY information from branch nodes. Jerry took the action item to research/resolve the following issues:

- required changes to root contention timings in support of long distance topologies
- required granularity of a link-based ping timer
- required timing specifications (either static or readable) of PHY/LINK interface if timer located within the link
- method of reporting min or max PHY_DELAYS from branch nodes.

Action Items

1. Eric Hannah to send Annex A and other isolation related edits to the editor
2. Rich Baker to document PHY-link reset problem and solution using LPS
3. Dave Wooten to provide drawings and text to document power distribution requirements as they pertain to safety
4. Peter Johansson to add the “generation bit” to the configuration ROM.
5. Brendan Traw to summarize CPTWG proposals on the reflector in early June
6. Prashant Kanhere to document the circumstances under which a PHY is expected to defer a register read request
7. Editor to add reference to P1394b draft specification.
8. Jerry Hauck to document required changes to root contention timings in support of long distance topologies
9. Joe Bennett to provide update LREQ table to editor
10. Jerry Hauck & Ganesh Murthy to clarify interaction of cycle synch with ack acceleration and to begin discussion of PHY power on defaults (with respect to accelerations) and necessary configuration bit(s).
11. Jerry Hauck to develop requested P1394a changes in light of a link based ping timer.

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